Designation: F 1892 – 98

AMERICAN SOCIETY FOR TESTING AND MATERIALS
100 Barr Harbor Dr., West Conshohocken, PA 19428
Reprinted from the Annual Book of ASTM Standards. Copyright ASTM

Standard Guide for Ionizing Radiation (Total Dose) Effects Testing of Semiconductor Devices[1]

This standard is issued under the fixed designation F 1892; the number immediately following the designation indicates the year of original adoption or, in the case of revision, the year of last revision. A number in parentheses indicates the year of last reapproval. A superscript epsilon (ε) indicates an editorial change since the last revision or reapproval.

INTRODUCTION

This guide is designed to assist investigators in performing ionizing radiation effects testing of semiconductor devices, commonly termed total dose testing. When actual use conditions, which includes dose, dose rate, temperature, and bias conditions and the time sequence of application of these conditions, are the same as those used in the test procedure, the results obtained using these test methods apply without qualification. For some part types, results obtained when following this guide are much more broadly applicable. There are many part types, however, where care must be used in extrapolating test results to situations that do not duplicate all aspects of the test conditions in which the response data were obtained. For example, some linear bipolar devices and devices containing metal oxide semiconductor (MOS) structures require special treatment. This guide provides direction for appropriate testing of such devices.

1. Scope

1.1 This guide presents background and guidelines for establishing an appropriate sequence of tests and data analysis procedures for determining the ionizing radiation (total dose) hardness of microelectronic devices for dose rates below 300 rd(SiO_2)/s. These tests and analysis will be appropriate to assist in the determination of the ability of the devices under test to meet specific hardness requirements or to evaluate the parts for use in a range of radiation environments.

1.2 The methods and guidelines presented will be applicable to characterization, qualification, and lot acceptance of silicon-based MOS and bipolar discrete devices and integrated circuits. They will be appropriate for treatment of the effects of electron and photon irradiation.

1.3 This guide provides a framework for choosing a test sequence based on general characteristics of the parts to be tested and the radiation hardness requirements or goals for these parts.

1.4 This guide provides for tradeoffs between minimizing the conservative nature of the testing method and minimizing the required testing effort.

1.5 Determination of an effective and economical hardness test typically will require several kinds of decisions. A partial enumeration of the decisions that typically must be made is as follows:

1.5.1 *Determination of the Need to Perform Device Characterization*—For some cases it may be more appropriate to adopt some kind of worst case testing scheme that does not require device characterization. For other cases it may be most effective to determine the effect of dose-rate on the radiation sensitivity of a device. As necessary, the appropriate level of detail of such a characterization also must be determined.

1.5.2 *Determination of an Effective Strategy for Minimizing the Effects of Irradiation Dose Rate on the Test Result*—The results of radiation testing on some types of devices are relatively insensitive to the dose rate of the radiation applied in the test. In contrast, many MOS devices and some bipolar devices have a significant sensitivity to dose rate. Several different strategies for managing the dose rate sensitivity of test results will be discussed.

1.5.3 *Choice of an Effective Test Methodology*—The selection of effective test methodologies will be discussed.

1.6 *Low Dose Requirements*—Hardness testing of MOS and bipolar microelectronic devices for the purpose of qualification or lot acceptance is not necessary when the required hardness is 100 rd(SiO_2) or lower.

1.7 *Sources*—This guide will cover effects due to device testing using irradiation from photon sources, such as ^{60}Co γ irradiators, ^{137}Cs γ irradiators, and low energy (approximately 10 keV) X-ray sources. Other sources of test radiation such as linacs, Van de Graaff sources, Dymnamitrons, SEM's, and flash X-ray sources occasionally are used but are outside the scope of this guide.

1.8 Displacement damage effects are outside the scope of this guide, as well.

1.9 The values stated in SI units are to be regarded as the standard.

---

[1] This guide is under the jurisdiction of ASTM Committee F-01 on Electronics and is the direct responsibility of Subcommittee F01.11 on Quality Hardness Assurance.

Current edition approved May 10, 1998. Published November 1998.

2. Referenced Documents

2.1 *ASTM Standards:*

E 170 Terminology Relating to Radiation Measurements and Dosimetry[2]

E 666 Practice for Calculating Absorbed Dose from Gamma or X Radiation[2]

E 668 Practice for the Application of Thermoluminescence-Dosimetry (TLD) Systems for Determining Absorbed Dose in Radiation-Hardness Testing of Electronic Devices[2]

E 1249 Practice for Minimizing Dosimetry Errors in Radiation Hardness Testing of Silicon Electronic Devices Using Co-60 Sources[2]

E 1250 Test Method for Application of Ionization Chambers to Assess the Low Energy Gamma Component of Cobalt-60 Irradiators Used in Radiation-Hardness Testing of Silicon Electronic Devices[2]

E 1275 Practice for Use of a Radiochromic Film Dosimetry System[2]

F 1467 Guide for Use of an X-Ray Tester (≈ 10 keV Photons) in Ionizing Radiation Effects Testing of Semiconductor Devices and Microcircuits[3]

2.2 *Military Specifications:*

MIL-STD-883, Method 1019, Ionizing Radiation (Total Dose) Test Method[4]

MIL-HDBK-814 Ionizing Dose and Neutron Hardness Assurance Guidelines for Microcircuits and Semiconductor Devices[4]

3. Terminology

3.1 For terms relating to radiation measurements and dosimetry, see Terminology E 170.

3.2 *Definitions of Terms Specific to This Standard:*

3.2.1 *accelerated annealing test*, *n*—procedure utilizing elevated temperature to accelerate time-dependent growth and annealing of trapped charge.

3.2.2 *category A*, *n*—used to refer to a bipolar part that is not low dose rate sensitive.

3.2.3 *category B*, *n*—used to refer to a bipolar part that is low dose rate sensitive.

3.2.4 *characterization*, *n*—testing to determine the effect of dose, dose-rate, bias, temperature, etc. on the radiation induced degradation of a part.

3.2.5 *gray*, *adj*—the gray (Gy) symbol, is the SI unit of absorbed dose, defined as 1 Gy = 1 J/kg (1 Gy = 100 rd).

3.2.6 *in-flux tests*, *n*—measurements made in-situ while the test device is in the radiation field.

3.2.7 *in-situ tests*, *n*—electrical measurements made on devices during, or before-and-after, irradiation while they remain in the irradiation location.

3.2.8 *in-source tests*, *n*—an in-flux test.

3.2.9 *ionizing radiation effects*, *n*—the changes in the electrical parameters of a microelectronic device resulting from radiation-induced trapped charge.

3.2.9.1 *Discussion*—Ionizing radiation effects are sometimes referred to as“ total dose effects.”

3.2.10 *low dose rate sensitive*, *adj*—used to refer to a bipolar part that shows enhanced radiation induced damage at dose rates below about 50 rd(SiO_2)/s.

3.2.10.1 *Discussion*—In this guide, doses and dose rates are specified in rd(SiO_2) as contrasted with the use of rd(Si) in other related standards. The reason is that for ionizing radiation effects in silicon based microelectronic components, it is the energy deposited in the SiO_2 gate, field, and spacer oxides that is responsible for the radiation-induced degradation effects. For high energy irradiation, for example, ^{60}Co photons, the difference between dose deposited in Si and SiO_2 typically is negligible. For X-ray irradiation, approximately 10 keV photon energy, the energy deposited in Si under some circumstances may be approximately 1.8 times the energy deposited in SiO_2. For additional details, see Guide F 1467.

3.2.11 *not in-flux test*, *n*—electrical measurements made on devices at any time other than during irradiation.

3.2.12 *qualification*, *n*—testing to determine the adequacy of a part to meet the requirements of a specific application.

3.2.13 *rad*, *n*—the rad symbol, rd, is a commonly used unit for absorbed dose, defined in terms of the SI unit of absorbed dose as 1 rd = 0.01 Gy.

3.2.14 *remote tests*, *n*—electrical measurements made on devices that are removed physically from the irradiation location for the measurements.

3.2.15 *time dependent effects (TDE)*, *n*—the time dependent growth and annealing of ionizing radiation induced trapped charge and interface states and the resulting transistor or IC parameter changes caused by these effects.

3.2.15.1 *Discussion*—Similar effects also take place during irradiation. Because of the complexity of time dependent effects, alternative, but not inconsistent, definitions may prove useful. Two of these are: the complex of time-dependent processes that alter trapped oxide change (ΔN_{ot}) and interface trap density (ΔN_{it}) in an MOS or bipolar structure during and after irradiation; and, the effects of these processes upon device or circuit characteristics or performance, or both.

4. Summary of Guide

4.1 This guide is designed to provide an introduction and direction to the purposes, methods, and strategies of total ionizing dose testing.

4.1.1 *Purposes*—Device or system hardness may be measured for several different purposes. These may include device characterization, device qualification, lot acceptance, line qualification, and studies of device physics.

4.1.2 *Methods*:

4.1.2.1 An ionizing radiation effects test consists of performing a set of electrical measurements on a device, exposing the device to ionizing radiation while appropriately biased, and then performing a set of electrical measurements either during or after irradiation.

4.1.2.2 Because several factors enter into the effects of the radiation on the device, parties to the test must establish and agree to a variety of conditions before the validity of the test can be established or before the results of any one test can be compared with those of another. Conditions that must be

[2] *Annual Book of ASTM Standards*, Vol 12.02.

[3] *Annual Book of ASTM Standards*, Vol 10.04.

[4] Available from the Standardization Documents Order Desk, Building 4, Section D, 700 Robbins Ave., Philadelphia, PA 19111–5094.

established and agreed to include the following:

(*a*) *Radiation Source*—The type of radiation source (^{60}Co, X-ray, etc.) that is to be used.

NOTE 1—The ionizing dose response of many device types has been shown to depend on the type of ionizing radiation to which the device is subjected. The selection of a suitable radiation source for use in such a test must be based on the understanding that the gamma or electron radiation source will induce a device response that then should be correlated to the response anticipated in the device application.

(*b*) *Dose Rate Range*—The range of dose rates within which the radiation exposures must take place (see 6.4).

NOTE 2—The response of many devices has been shown to be highly dependent on the rate at which the dose is accumulated. There must be a demonstrated correlation between the response of the device under the selected test conditions and the rate at which the device would be expected to accumulate dose in its intended application.

(*c*) *Operating Conditions*—The test circuit, electrical biases to be applied, and the electrical operating sequence, if applicable, for the part during irradiation (see 6.3). This includes the use of in-flux or not in-flux testing.

(*d*) *Electrical Parameters*—The measurements that are to be made on the test devices before, during (if appropriate), and after (if appropriate) irradiation.

(*e*) *Time Sequence*—The exposure time, the elapsed time between exposure and post-exposure measurements, and the time between irradiations (see 6.5).

(*f*) *Irradiation Levels*—The dose(s) to which the test device is to be exposed between measurements (see Practice E 666).

(*g*) *Dosimetry*—The dosimetry technique (TLDs, calorimeters, diodes, etc.) to be used. This depends to some extent on the radiation source selection.

(*h*) *Temperature*—Exposure, measurement, and storage temperature ranges (see 6.5 and 6.6).

(*i*) *Experimental Configuration*—The physical arrangement of the radiation source, test unit, radiation shielding, and any other mechanical or electrical elements of the test.

(*j*) *Accelerated Annealing Testing for MOS*—The accelerated annealing tests called for in 8.2.2.3 (*a*) through (*e*) should be performed for hardness assurance testing of any device that contains MOS elements by design. Further requirements and exceptions to such accelerated annealing testing may be made based on the factors discussed in Appendix X1.

(*k*) *Special Testing for Linear Bipolar* — The special testing procedures called for in 8.1.2.1 through 8.1.2.4 (*e*), and 8.2.3.1 through 8.2.3.4 should be performed for hardness assurance testing of linear bipolar devices. Further requirements and suggestions for the testing of linear bipolar devices will be found in Appendix X2.

4.1.3 *Strategies*—Several kinds of strategies may prove useful for device testing. The strategy used will depend on the key impediments to accurate, repeatable, and inexpensive testing. For example, it may be useful to measure device properties at several different dose rates and then to extrapolate to the results expected at the actual dose rate anticipated in use. Then again, it may be more efficient to devise a method that will place an upper or lower bound on the excursions that may be anticipated for a given device parameter.

4.2 The choice of optimal procedures for the performance of total ionizing dose testing typically involves resolution of the conflicts between the following four competing requirements:

4.2.1 *Test Fidelity*—It is necessary that a test reproduce the results to be expected in the projected application environment to an acceptable degree of precision. The test methodology chosen has a strong effect on the precision of the result. Typically, however, greater test fidelity must be balanced against greater cost. In addition, many environments cannot be reproduced in the laboratory. Often it may be necessary to have an adequate command of device physics in order to devise laboratory tests that adequately match or bound the performance to be expected in actual use.

4.2.2 *Reproducibility*—It is important to have test procedures that can be depended upon to give approximately the same result each time when used by different laboratories. Failure to achieve this goal may have significant contract implications. Obtaining this goal typically requires careful attention to the control of experimental variables and to the development of accurate dosimetry methods.

4.2.3 *Single-Valued Result*—For some purposes, it is desirable to have a test that can be used to simply categorize parts and that gives one answer for each part. For example, labeling of parts for the military parts system is facilitated if such a characterization is available. On the other hand, the search for a simple characterization scheme must not be allowed to obscure real dependencies on dose rate, temperature, bias, etc., which may have a significant effect on operational hardness. Care must be taken to extrapolate appropriately from the conditions that lead to the test rating to those conditions to be expected in use.

4.2.4 *Testability*—It is, of course, desirable to obtain a test that is economical in its use of time, equipment, and personnel. The perfect test typically will be too expensive to perform. The goal is to determine an optimal balance between expense and reliability of results.

5. Significance and Use

5.1 Electronic circuits used in space, military, and nuclear power systems may be exposed to various levels of ionizing radiation. It is essential for the design and fabrication of such circuits that test methods be available that can determine the vulnerability or hardness (measure of nonvulnerability) of components to be used in such systems.

5.2 Some manufacturers currently are selling semiconductor parts with guaranteed hardness ratings. Use of this guide provides a basis for standardized qualification and acceptance testing.

6. Interferences

6.1 There are many factors that can affect the results of ionizing radiation tests. Care must be taken to control these factors to obtain consistent and reproducible results. Several of these factors are discussed as follows:

6.2 *Energy Spectrum*—Many gamma-ray sources have associated low-energy electron and photon components that result from interaction of the gamma radiation with shielding surrounding the source (see Practice E 1249). These low-energy components can deposit their energy in a shallow layer near the surface of the device chip. This places an absorbed

dose in the most susceptible region of a test device that can be much higher than the dose measured by a monitoring dosimeter, typically the average dose deposited in the dosimeter material. The severity of the effects is very dependent on the radiation source being used and the geometry of the test configuration.

6.3 *Bias*—Most ionizing radiation effects are related to the post irradiation net trapped charge in the device dielectric layers, usually oxides, and to the interface traps at the dielectric-semiconductor interface. These effects often are dependent strongly on the electrical field in the dielectric during and after exposure (see Test Method E 1250). In general, the largest effect for the net trapped charge occurs for a large positive electric field in the dielectric during irradiation. For the interface trap build-up, the worst case condition most often is a small electric field during irradiation and a large positive field after irradiation. Radiation testing typically is performed under worst-case bias conditions. For many circuits, the worst-case bias is a static dc bias with the supply voltages at their maximum rated voltage. The determination of the worst case bias for the input/output lines and internal nodes of any given circuit often is a complex process of circuit analysis or characterization tests, or both, under many bias conditions. Some guidance is given in the appendices for methods to determine the worst case irradiation and anneal bias. For complementary metal-oxide semiconductor transistor (CMOS) components, see Appendix X1; for bipolar components, see Appendix X2; and, for application-specific integrated circuits, (ASIC) see Appendix X3. The irradiation bias conditions selected for any component should not exceed the manufacturer's maximum ratings or place the component in a configuration that is unrealistic for a system application.

NOTE 3—Lacking information on worst-case application conditions, preliminary analysis and characterization tests should be performed to determine worst-case conditions. In performing step-wise irradiations, it is important to minimize the changes taking place between exposures so that measurements at each level accurately reflect the effects of the cumulative dose to which the device was exposed. Minimum parameter changes generally take place between exposures if the device pins are kept shorted. Bias should not be changed from one level to another in a step stress sequence, in order to avoid charge neutralization effects.

NOTE 4—Some space applications involve devices used at very low repetition rates; for example, electrically programmable read-only memory (EPROM's.) Another example is redundant devices and circuits that ride along in an unbiased condition until they are switched on. Still another example is sensor circuits that only are biased on when a measurement is to be taken. Thus, it may be desirable to characterize and test these devices in an unbiased condition. Ionizing dose survival levels may be three to ten times higher in the unbiased condition than under typical bias conditions.

6.4 *Dose Rate*:

6.4.1 The concentration of excess carriers depends on the dose rate. High densities of excess carriers can affect the charge state of trapping levels, as well as the mobilities and lifetimes of these carriers resulting in altered post-radiation densities and distributions of trapped charge.

6.4.2 Photocurrents produced by the excess carriers generated by ionization can alter internal bias levels of a semiconductor chip, thereby causing a variation in the response of the device or circuit.

6.4.3 Because of the counteracting effects of charge annealing and interface state growth in some MOS device oxides, the dose rate at which a test is carried out can have a strong effect on the apparent device hardness (see 6.5 for further detail).

6.4.4 For the reasons noted in 6.4.1-6.4.3, the dose rate to be used in an ionizing radiation test must be established and agreed upon between the parties to the test and controlled during the test. Selection of appropriate dose rate ranges should be based on the radiation environments anticipated for the parts while in actual system operation.

6.4.5 The use of thick absorbers in order to produce a low dose-rate ^{60}Co test source must be used with caution. The absorbers may cause softening of the spectrum (through Compton scattering). This may cause dose deposition and dose enhancement problems (see 6.2).

6.5 *Time Dependent Effects*:

6.5.1 *Time Dependent Effects for MOS Devices*:

6.5.1.1 Ionizing irradiation of MOS devices results in two major species of defects: trapped holes in gate (and field) oxides and interface states at $Si\text{-}SiO_2$ interfaces. Hole trapping occurs rapidly (typically less than ~1 s) and often anneals significantly in hours or days. Interface state density builds up slowly (in seconds to days) and does not usually anneal significantly at room temperature. The relative magnitudes of these defects determine the effects on operation of the device and its post-irradiation time dependence. The quality of the oxide determines the relative densities and saturation levels of the defects.

6.5.1.2 Trapped holes in the silicon oxide result in a negative shift in the gate threshold voltage for both *n*- and *p*-channel devices. Interface states maintain a net negative charge in *n*-channel devices (positive gate threshold shift) and a net positive charge in *p*-channel devices (negative gate threshold shift).

6.5.1.3 With increasing time, trapped holes are removed or compensated while interface state concentrations increase. Because hole trapping occurs rapidly, initial gate threshold shifts in both *p*- and *n*-channel devices are negative under irradiation at moderate to high dose rates. As time passes, the gate threshold shift of *n*-channel devices becomes less negative, and, if interface states build up sufficiently, can eventually become positive. Whether *p*-channel gate shifts become more or less negative with time depends on the relative rates of formation of interface states and the removal of trapped holes, but the shift always remains negative.

6.5.1.4 The interaction of these competing effects that shift with time cause the sometimes complex time dependent behavior of MOS parts following irradiation. This complex behavior explains observed effects once thought anomalous: reverse annealing, in which parts continue to degrade with time following cessation of irradiation; the rebound effect, in which *n*-channel devices super-recover past their preirradiation gate threshold values and can fail due to a positive gate threshold shift; dose rate effects where parts show little change at a particular dose rate but show a significant response at either higher or lower dose rates (because at the intermediate dose rate the net oxide-trapped charge buildup is balanced by interface buildup); etc.

6.5.2 *Time Dependent Effects for Bipolar Devices*:

6.5.2.1 The crux of the bipolar TDE issue concerns the properties of spacer oxides used to isolate the base and emitter contacts. These oxides typically are of poor quality. The effects of radiation on such oxides determine the radiation response of many bipolar transistors. A characteristic failure mechanism in such bipolar transistors is radiation-induced increase in the base current, and resulting decrease in transistor gain. This excess base current largely is caused by enhanced surface recombination current in the emitter-base diode.

6.5.2.2 For the bipolar technologies mentioned above, failures occur at lower doses for irradiations at low dose rates than at higher rates. For example, the devices may show higher excess base currents below 1 rd(SiO_2)/s than at 100 rd/(SiO_2)/s, for the same level of accumulated total ionizing dose. Such enhanced failure at low dose rates has been observed both in modern bipolar technologies and in relatively old designs. These effects have been observed both in transistors and ICs.

6.5.2.3 These low dose-rate effects often cannot be simulated by accelerated anneal procedures, such as that recommended for MOS devices in 8.2.2.3 (*a*) through (*e*) and Appendix X1. Currently, there is no proven single method for accelerating the testing of low dose-rate irradiation for all types of dose-rate sensitive bipolar devices. Some promising test methods, however, are described in Appendix X2.

6.6 *Temperature*:

6.6.1 Because time-dependent effects (see 6.5) may be thermally-activated processes, the temperatures at which radiation, measurements, and storage take place can affect parameter values. It is recommended that all radiation exposures, measurements, and storage be done at 24 ± 6°C unless another temperature range is called out specifically in the test or is agreed upon between the parties to the test. If devices are to be transported to and from a remote electrical measurement site, the temperature of the devices shall not be allowed to increase by more than 10°C from the radiation-environment temperature.

6.6.2 Many device parameters are temperature sensitive. To obtain accurate measures of the radiation-induced parameter changes, the temperature must be controlled.

6.6.3 Temperature effects also must be considered in establishing the sequence of post-irradiation testing. The sequence of parameter measurements should be chosen to allow lowest power dissipation measurements to be made first. Power dissipation may increase with each subsequent measurement. When high power is to be dissipated in the test devices, pulsed measurements are required to minimize the temperature excursions.

6.7 *Handling*—As in any other type of testing, care must be taken in handling the parts. This applies especially to parts that are susceptible to electrostatic discharge damage.

6.8 *Delidding*—For some testing, it is necessary to de-lid the devices prior to irradiation and testing. Care must be taken to make proper allowance for the effects of such a process.

6.9 *Radiation Damage*:

6.9.1 If a test fixture is used over a long period of time, components of the fixture can be damaged by exposure to the ionizing radiation, causing an impact on the test results. Such fixtures should be checked regularly for socket or printed circuit board leakage and for degradation of any peripheral components used in the test. Current leakage between pins or wires shall not be allowed to approach levels that interfere with accurate parameter measurements.

6.9.2 Ionizing radiation causes the introduction of color centers in optical materials, seriously degrading light transmission properties. Much of the radiation damage to devices containing optical elements may be due to this effect rather than to damage of the semiconductor elements. Such damage to the device under test or to test circuitry is outside the scope of this guide.

6.10 *Burn-In*—Burn-in is a set of elevated-temperature biased anneals required by reliability testing and the system application. For some devices, there is a significant difference in the radiation response before and after burn-in. Unless it has been shown by characterization testing that burn-in has no effect on radiation response, then either characterization and qualification testing must be performed on devices that have been exposed to all elevated-temperature biased (or unbiased) anneals required by reliability testing and the system application, or the results of characterization and qualification testing must be corrected for the changes in radiation response that would have been caused by elevated temperature anneals (such as burn-in). This correction shall be performed in a manner acceptable to the parties to the test.

6.11 *Test Sample Size*—There is a difficult trade-off in deciding the number of devices to use for a particular test. Using a large number may in some cases be prohibitively expensive. Then again, the reliability of a test result may be unacceptably low if too small a sample size is used. This outcome results from part-to-part variability within a given test lot. The sample sizes specified in this guide are accepted generally in the industry.

7. Apparatus

7.1 *Radiation Sources Used for Ionizing Radiation (Total Dose) Effects Testing*:

7.1.1 Sources typically used for characterization, qualification and lot acceptance testing include ^{60}Co and ^{137}Cs isotopes (mounted in pool sources, pop-up sources, and fully shielded irradiators), and low energy (approximately 10 keV photon energy) X-ray sources.

7.1.1.1 Each source can be used satisfactorily for such tests, and the differences in the results from using different sources or kinds of sources should be negligible provided that dose rates can be matched or deemed to have no significant impact on the devices being tested.

7.1.1.2 The radiation environment impinging on the tested device must be characterized in terms of photon energy spectrum and dose rate. In situations where the photon energy spectrum impinging on the device is not or cannot be well defined, but is suspected to contain low energy components that promote absorbed dose enhancement, a filter box such as the lead-aluminum structure (see 7.1.2.1 and Practice E 1249) can be incorporated into the radiation test environment to harden the photon spectrum.

7.1.2 The following radiation sources may be used to support ionizing radiation effects testing:

7.1.2.1 ^{60}*Co*—The most commonly used source for ionization radiation (total dose) effects testing is ^{60}Co. Gamma rays with energies of 1.17 and 1.33 MeV are the primary ionizing radiation emitted by ^{60}Co (see 6.2). In exposures using ^{60}Co sources, test specimens must be enclosed in a lead-aluminum container to minimize dose enhancement effects caused by low-energy scattered radiation. A minimum of 1.5 mm of lead surrounding an inner shield of 0.7 to 1.0 mm of aluminum is required. This lead-aluminum container produces an approximate charged particle equilibrium for silicon devices with some attenuation of the gamma rays. Because of this attenuation, the gamma ray intensity inside the container shall be calibrated initially, whenever sources are changed, and each time the source, container, or test fixture orientation or configurations are changed. This measurement shall be performed by placing a dosimeter, for example a TLD, in the device irradiation container at the approximate position of the test device (see Practice E 1249).

7.1.2.2 ^{137}*Cs*—Radiation sources based on ^{137}Cs can be used for characterization testing in much the same way as ^{60}Co sources.

7.1.2.3 A special case of radioactive source testing, for example, ^{60}Co sources and ^{137}Cs sources, is to support very low dose rate testing, that is, $<$1 rd/s. The use of attenuation to obtain a low dose rate, for example the use of lead bricks or sheet, can add a significant low energy component to the radiation due to Compton scattering. The radiation effects of such a softened beam may be significantly different than those of the unattenuated beam. See Practice E 1249 for additional discussion. Special care is required to support such testing.

7.1.2.4 *Low Energy X-Ray Source*—Low energy (approximately 10 keV photon energy) X-ray sources commonly are used for transistor characterization. Because of the low penetration of such photons, devices must be tested prior to packaging or be delidded for testing. For additional detail, see Guide F 1467.

7.2 *Bias Circuit*—The bias circuit may be simple or complex, depending on the part type and testing requirements. Good commercial design and fabrication practices should be used to prevent oscillations, minimize leakage currents, prevent device damage, and support accurate and repeatable measurements. For test fixtures holding several devices, isolation should be used between devices so that a failure of one device will not impact the other test units. For in-situ measurements, provision must be made for switching individual devices between the radiation bias circuit and the test instrumentation used for pre- and post-irradiation parameter measurements. For remote measurements, MOS and bipolar parts should be maintained with shorted leads during transport.

7.3 *Test Instrumentation*—Various instruments for device parameter measurement may be required. Depending upon the device to be tested, these can range from simple broadboard circuits to complex IC test systems. All equipment is to be in calibration and of suitable stability and accuracy.

7.4 *Dosimetry System*:

7.4.1 *Determination of Absorbed Dose*—Determining the absorbed dose in a semiconductor device requires a knowledge of the elemental composition and geometrical structure of the materials involved, the appropriate tabulated[5] mass energy-absorption coefficients (μ_{en}/ρ), the energy spectrum of the radiation field (not merely that of the unperturbed radiation source, in which the exposure is conducted), and a related measurement based on a dosimeter whose response is well defined in the particular radiation field of interest.

7.4.2 For ^{60}Co irradiation systems, dosimetry most often is performed using thermoluminescent dosimeters (TLDs) to measure the dose inside the lead-aluminum container delivered in a fixed time period. Other dosimeters, such as cobalt glass, radiochromic dye dosimeters (see Practice E 1275), or ion chambers, however, can be used. This measurement is used to establish the dose rate for the geometry used. Once the dose rate is established, preselected radiation levels are attained by irradiating for the proper time period. TLDs also may be used with any of the other radiation sources. Dosimeter systems can be calibrated through a service of the NIST.[6] Proper use of TLD systems is described in Practice E 668.

7.5 *Irradiation Temperature Chamber*—Ionizing radiation effects testing may require the use of an elevated temperature irradiation chamber (see 8.1.2.1 (*d*) (*2*), 8.1.2.2 (*b*) (*1*), 8.1.2.4 and 8.2.3.3 (*b*).

8. Procedure

INTRODUCTION

This section provides guidance for characterization testing and for hardness assurance acceptance testing.

NOTE 5—Hardness assurance refers to part qualification and lot/process quality conformance.

NOTE 6—*Semiconductor Devices and Integrated Circuits with Intended Use at Dose Rates above 300 rd (SiO_2)/s*—For some strategic and possibly some tactical military applications, the ionizing dose response of many semiconductor devices can be non-monotonic with the severity of non-monotonic behavior depending strongly on both ionizing dose and dose rate. This problem can occur for ionizing dose in the prompt pulse resulting from a nuclear explosion. Parameters, such as leakage currents and current gain, may reach failure levels during the pulse and return to passing levels shortly after the pulse. The time during which the parameters are above failure level may cause system failure even though they return to passing levels after a short period of time. Hardness assurance testing for these parts is discussed in Appendix X1.

8.1 *Characterization Testing*—Characterization testing is performed for the purpose of part selection, determination of sensitivity to dose rate or time dependent effects, categorization for hardness assurance, or to determine the specific nominal worst case test conditions for hardness assurance testing.

8.1.1 *MOS Devices and Integrated Circuits with Intended Use At Dose Rates At or Below 300 rd(SiO_2)/s*—Parts in this category are those intended for use in, for example, space

[5] See, for example, Hubbell, J.H. and Seltzer, S.M. "Tables of X-Ray Mass Attenuation Coefficients and Mass Energy-Absorption Coefficients, 1 keV to 20 MeV for Elements Z = 1 to 92 and 48 Additional Substances of Dosimetric Interest," *NISTIR 5632*, May 1995. Available from Ionizing Radiation Division, Physics Laboratory, National Institute of Standards and Technology, Technology Administration, U.S. Department of Commerce, Gaithersburg, MD 20899.

[6] To schedule calibration services, contact Center for Radiation Research, Radiation Physics Building, National Institute of Standards and Technology (NIST), Gaithersburg, MD 20899.

systems, some tactical military systems, some nuclear power plant electronics or associated robotics, and high energy particle accelerator detectors.

8.1.1.1 Parties to the test must first establish the conditions of the test. These conditions should be stated in a test plan as follows:

(*a*) *Development of the Test Plan*—As a minimum, the following conditions should be specified: test approach (step-stress or continuous), test type (in-flux, in-situ, or remote), irradiation source, total dose levels for electrical measurements (for step-stress), dose rate(s), irradiation bias(es), irradiation temperature(s), anneal bias(es), anneal temperature(s), anneal times, and use of test structures (where appropriate). In addition, it may be appropriate to specify date code information for the test devices (that is, limitations on the number of diffusion furnace lots or time to assemble date code lot, or both). All of the possible interferences listed in Section 6 must be considered when making these decisions.

(*b*) *Dose Rate*—The dose rate for the test shall be selected from one of the following possibilities:

(1) Standard Dose Rate, Condition A—Unless otherwise specified, the dose-rate range shall be between 50 and 300 rd(SiO_2)/s. The dose rates may be different for each radiation dose level in a series; however, the dose rate shall not vary by more than ± 10 % during each irradiation.

(2) Condition B—As an alternative, the test may be performed at the dose rate of the intended application if this is agreed to by the parties to the test.

(3) Condition C—As an alternative, if the maximum dose rate is < 50 rd(SiO_2)/s in the intended application, the parties to the test may agree to perform the test at a dose rate ≥ the maximum dose rate of the intended application.

(4) Condition D—To meet unusual requirements and if agreed upon between the parties to the test, a dose rate that fits none of the above conditions may be used.

(*c*) *Sample Selection*—The sample size for each unique set of test conditions should be at least five and preferably larger. The total population from which the test sample is drawn will depend on the purpose of the characterization. For example, if the parts are to be used in a system, the population should be representative of the parts that will be used for flight hardware, that is, single wafer, single process lot, single date code, or multiple lots. If multiple lots are allowed, as a minimum the test sample should contain parts from at least three date codes or process lots. Control devices from the same population as the test samples should be employed to monitor repeatability of electrical test parameters.

(*d*) *Development of Test Matrix*—For many of the test conditions there will be several values, for example, two or more irradiation biases, two or more dose rates, two or more annealing temperatures. If all of these test conditions are to be exercised with respect to all of the others, that is, a full factorial matrix, then the total sample size (for a minimum sample of five for each element) may be unmanageable. In this case, it is recommended that a reduced matrix be used. Best engineering judgment must be used in selecting the most important test parameters to emphasize. The test matrix should be included in the test plan.

8.1.1.2 Start with the first element (unique set of test conditions) in the test matrix. Prepare bias fixtures, test fixtures, test circuits (or test equipment), and test programs.

8.1.1.3 Perform dosimetry, including dose mapping of the entire device irradiation area, if recent data for such measurements are not available. For ^{60}Co irradiation, the dosimetry must be performed inside the lead-aluminum shield box (Section 7). Determine appropriate factors to convert dose in the dosimeter to dose in the device under test using Practice E 666.

(*a*) As an exception to 8.1.1.3, the lead-aluminum shield box, may be omitted for the dosimetry and the subsequent test sample irradiations under appropriate circumstances. In order to make this omission, it must be demonstrated that dose enhancement inside the test sample package is negligible for the irradiation source being used (see Test Method E 1250).

8.1.1.4 If the devices are being tested in-flux using the continuous irradiation approach, place the devices in the irradiation test circuit inside the lead-aluminum shield box, if used, and initiate the test circuit. Record the preirradiation parameter, or functional measurements, or both. Begin irradiating the parts at the prescribed dose rate and continue to monitor the electrical parameters/functionality of the devices, either continuously or at the prescribed time intervals, until the final dose level is reached or the parts become nonfunctional. Assure that all electrical data are time stamped so that the total dose levels for each set of measurements may be calculated.

8.1.1.5 If the devices are being irradiated using the step-stress approach, begin by making preirradiation parameter, or functional measurements, or both. Place the parts in the irradiation bias fixture in the lead-aluminum shield box, if used, and irradiate to the first total dose level. Perform the post irradiation electrical measurements either in-situ or at a remote site. If testing is remote, the parts should be transported to and from the test equipment with shorted leads. Conductive foam may be used to accomplish this shorting. Replace the parts in the irradiation bias fixture and irradiate to the next total dose level, following the same procedure just described, until the final level is reached. The time between irradiation and test and the time between irradiations should be minimized and recorded.

8.1.1.6 Following the final irradiation, post-irradiation annealing measurements shall be made if required by the test plan. Annealing measurements usually are made using a step-stress approach. Time zero for the annealing should be set immediately following the final postirradiation electrical characterization or when bias is applied (for biased anneals). Annealing may be performed at room temperature or at an elevated temperature as prescribed by the test plan. All electrical measurements shall be made at room temperature (24±6°C) unless otherwise specified by the test plan. See the following for use of an accelerated annealing procedure:

(*a*) For details of the use of an accelerated annealing procedure to simulate space-level low dose rate effects, see 8.2.2.3, (*a*) through (*f*). Such a procedure may be required for hardness assurance testing. It also may be performed for characterization testing if prescribed by the test plan. Additional guidance may be found in Appendix X1.

(*b*) If the anneals are to be performed at room temperature, the test devices shall be placed in the anneal bias fixture, the bias applied, and the parts left for the prescribed period. The parts then shall be characterized electrically either in-situ or at a remote site. Transport to and from a remote test site shall be with shorted leads. Conductive foam may be used to accomplish this shorting. This procedure shall be repeated until the final anneal time prescribed by the test plan is reached. The time between anneal and electrical characterization and the time between anneals shall be minimized and recorded. The temperature of the anneal shall be recorded.

(*c*) If the anneals are to be performed at an elevated temperature, the test devices shall be placed in the anneal bias test fixture inside the environmental chamber, the bias applied, and the temperature rapidly brought to the anneal temperature and maintained for the first anneal time. The temperature then shall be reduced rapidly to room temperature while maintaining bias, and the parts characterized electrically, either in-situ, or at a remote test site, as prescribed in the test plan. If the testing is to be performed at a remote site, the parts shall be transported to and from the anneal chamber with shorted leads. Conductive foam may be used to accomplish this shorting. This procedure shall be repeated until the final elevated temperature anneal time prescribed by the test plan is reached. The elevated temperature anneal time shall be calculated without regard to time at room temperature during test sequences. The time between anneal and electrical characterization and the time between anneals shall be minimized and recorded.

8.1.1.7 The procedures described in 8.1.1.2-8.1.1.6 shall be repeated for each element of the matrix.

8.1.2 *Bipolar Devices and Integrated Circuits with Intended Use at Dose Rates At or Below 300 rd(SiO_2)/s*—Parts in this category are those intended for use in, for example, space systems, some tactical military systems, nuclear power plants or associated robotics, and high energy particle accelerator detectors.

8.1.2.1 *Dose Rate Sensitivity*:

INTRODUCTION

(*a*) It has been demonstrated that several bipolar linear circuits exhibit an increased rate of degradation at low dose rates (see Appendix X2.2.2). The effect is such that if we compare gain degradation for two cases: at the end of a low dose rate exposure, and at the end of a high dose rate exposure to the same dose, followed by a room temperature anneal for the same time as it takes for the low dose rate exposure, the gain degradation for first case can be much greater. This effect will be referred to as "dose rate sensitivity".

NOTE 7—Low dose rate sensitivity on discrete bipolar transistors has not yet been observed to be greater than a factor of two. Also, it has not been observed on any type of MOS transistor while under normal operating bias.

(*b*) The first concern for characterization testing for bipolar parts is to identify low dose rate sensitive parts. Parts, which are not low dose rate sensitive, are classified as Category A Parts and parts, which are low dose rate sensitive, are classified as Category B Parts. A set of tests to determine whether a device-under-test is Category A or Category B is described in 8.1.2.2. If previous testing on the same or similar parts has indicated that these parts are low dose rate sensitive, the devices-under-test may, with the agreement of the parties to test, be classified as Category B and the tests of 8.1.2.2 may be skipped.

(*c*) *Testing Parts Which Are Not Low Dose Rate Sensitive*—For parts that are not low dose rate sensitive, the characterization testing may be performed at the standard dose rate of 50 to 300 rd(SiO_2)/s (see 8.1.1.1 (*b*) (*1*)).

(*d*) *Testing Parts Which Are Low Dose Rate Sensitive:*

(*1*) Low dose rate sensitive parts may be tested at the dose rate of the intended application; however, this often may be impractical.

(*2*) For low dose rate applications, in many cases it will be desirable to use an accelerated testing method; that is, a test method that provides a conservative measure of low dose rate part response while using test irradiation at a dose rate well above that expected in the intended application. Some combination of overtest, elevated temperature irradiation and anneal, can bound the low dose rate response for many low dose rate sensitive parts. If a part is low dose rate sensitive and is to be used in a low dose rate application, the determination of an appropriate accelerated test method for a given test typically will involve characterization over a range of dose rates to select test procedures that will bound the low dose rate response.

NOTE 8—Based on transistor and base oxide capacitor tests, initial studies of the mechanisms of the low dose rate sensitivity have suggested that an elevated temperature irradiation at ~ 10–100 rd(SiO_2)/s can produce comparable damage to a low dose rate exposure in some cases. Also, it has been shown that an extended room temperature anneal following high dose rate irradiation may result in additional degradation in some circuits, particularly those which fail from gain degradation in a substrate or lateral pnp.

8.1.2.2 *Test to Determine Low Dose Rate Sensitivity*—Before proceeding with the full characterization testing, a preliminary screen test should be run to determine whether the bipolar part has enhanced degradation at low dose rates, unless the dose rate sensitivity already has been determined through previous testing or analysis. This preliminary test should be run on all bipolar microcircuits which contain linear circuitry and any discrete or digital part which is suspected of being dose rate sensitive (see Appendix X2 for discussion). The test for dose rate sensitivity may be run either at two dose rates for irradiation at room temperature (RT), (see 8.1.2.2 (*a*)) or at two irradiation temperatures for a dose rate of 50 to 300 rd(SiO_2)/s, (see 8.1.2.2 (*b*)).

(*a*) *Dose Rate Sensitivity Test at Two Dose Rates*—From a population representative of the end use application of the characterization test results, randomly select a minimum of 20 parts. Smaller sample sizes may be used if agreed upon between the parties to the test. All of the selected devices shall have undergone appropriate elevated temperature reliability screens.

NOTE 9—There are risks involved in using smaller numbers of test parts. These result from part-to-part variability within a given test lot.

NOTE 10—Low dose rate sensitivity often has been observed to show a large variability in response with a change in date code.

(*1*) Divide the test sample into two equal groups of at least ten and irradiate one group at a dose rate of 50 to 300

$rd(SiO_2)/s$, and the other group at a dose rate of 0.02 to 0.1 $rd(SiO_2)/s$ (the ratio of the high dose rate to low dose rate shall be at least 1000). Perform the irradiation and test as follows:

(*2*) Prepare bias fixtures, test fixtures, test circuits (or test equipment), and test programs.

(*3*) The irradiation shall be performed using a ^{60}Co or ^{137}Cs irradiation source.

(*4*) Conduct the irradiation and dosimetry as specified in 8.1.1.3-8.1.1.5.

(*5*) Special care is required if radiation beam attenuation is used in order to reduce the experimental dose rate (see 7.1.2.3).

(*6*) Compare the median values of the radiation induced change of the most sensitive parameters at each of the dose levels tested. If the ratio of the median value at low dose rate to the median value at high dose rate is > 1.5, the part is considered to be a Category B (low dose rate sensitive) part. Low dose rate sensitive parts shall be tested at the intended use dose rate or subjected to characterization testing to develop a hardness assurance procedure that will bound the low dose rate response (see Appendix X2 for recommendations).

(*b*) *Dose Rate Sensitivity Test at Two Irradiation Temperatures*—From a population representative of the end use application of the characterization test results, randomly select a minimum of 20 parts. Smaller sample sizes may be used if agreed to by the parties to the test. All of the selected devices shall have undergone appropriate elevated temperature reliability screens.

(*1*) Divide the test sample into two equal groups of at least ten and irradiate one group at a an irradiation temperature of 125±5°C and the other group at an irradiation temperature of 24±6°C. Perform the irradiation and test as follows:

(*2*) Prepare bias fixtures, test fixtures, test circuits (or test equipment), and test programs.

(*3*) Perform dosimetry and irradiation as specified in 8.1.1.3, and 8.1.1.3 (*a*).

(*4*) Special care is required if radiation beam attenuation is used in order to reduce the experimental dose rate (see 7.1.2.3).

(*5*) The devices shall be irradiated using the step-stress approach beginning with preirradiation parameter, or functional measurements, or both, at room temperature. For the parts being irradiated at room temperature, conduct the irradiation as specified in 8.1.1.5. For the parts being irradiated at elevated temperature, place the parts in the irradiation fixture in the environmental irradiation chamber (see Section 7), rapidly heat the test samples to the required temperature and stabilize for no more than three minutes before irradiation. Irradiate to the first total dose level, rapidly reduce the temperature to room temperature and stabilize for at least three minutes. Perform the electrical characterization either in-situ or at a remote site. If testing is remote, the parts should be transported to and from the test with shorted leads. Conductive foam may be used to accomplish this shorting. Repeat the procedure just described to the next required dose level until the final total dose is reached.

(*6*) Compare the median values of the radiation induced change of the most sensitive parameters at each of the dose levels tested. If the ratio of the median value at elevated temperature to the median value at room temperature is > 1.5, the part is considered to be a Category B (low-dose-rate sensitive) part. Low-dose-rate sensitive parts shall be tested at the intended use dose rate or subjected to characterization testing to develop a hardness assurance procedure that will bound the low dose rate response (see Appendix X2 for recommendations).

8.1.2.3 *Characterization Testing of Category A Parts*—The characterization of Category A bipolar parts shall follow the same procedures as prescribed for MOS parts (see 8.1.1.1-8.1.1.7). The dose rate for these tests shall be the standard dose rate of 50 to 300 $rd(SiO_2)/s$ (see 8.1.1.1 (*b*) (*1*) or MIL-STD-883, Test Method 1019) unless otherwise required by the test plan.

8.1.2.4 *Characterization Testing of Category B Parts*:

(*a*) One of the main objectives of the Category B characterization testing is to determine the dose rate response of the parts down to dose rates of interest for the intended use. Fortunately, most low-dose-rate sensitive parts show a saturation of the enhanced response at dose rates below a value determined by the most sensitive transistor type for the parameter of interest. For some part types, this may be ~ 1 $rd(SiO_2)/s$, and for others it may be ~ 1–10 $mrd(SiO_2)/s$.

(*b*) The characterization testing should be performed over a range of dose rates starting at ~ 100 $rd(SiO_2)/s$ and going to dose rates sufficiently low to observe saturation of the enhanced response. An exception to this rule is that the testing need not be carried down to dose rates below that specified for the intended use of the device-under-test if this is agreed to by the parties to the test. If no saturation is observed at practically attainable dose rates, engineering judgement is required, for example, via use of overstress and extrapolation techniques, to estimate saturated values.

(*c*) Once the dose rate response has been determined, further characterization should be performed to establish practical test procedures that will bound the low dose rate response (see Appendix X2 for discussion). These tests may include elevated temperature irradiations. The characterization testing of Category B parts, therefore, should follow the same procedures as described in 8.1.1.1-8.1.1.7 with the addition of the following paragraph:

(*d*) If the devices are to be irradiated at an elevated temperature, follow the procedures in 8.1.1.2 through 8.1.1.5 as well as the next statement. After electrical characterization and before each irradiation begins, the test devices shall be heated rapidly to the prescribed temperature and stabilized for no more than three minutes before irradiation. See Section 7 for a description of the environmental irradiation chamber. At the end of each irradiation, the temperature shall be reduced rapidly to room temperature and stabilized for at least three minutes before electrical characterization.

(*e*) For discussion of the possible elevated temperature irradiation procedures for use in hardness assurance testing, see 8.2.3.3 (*b*) and Appendix X2.

8.2 *Hardness Assurance Acceptance Testing*—Hardness assurance testing is performed for qualification or lot/process quality conformance, often for a specific system application. Hardness assurance testing will be performed using a prescribed method of test sample selection and a single set of test

conditions, such as irradiation bias, dose rate, and total dose levels. The specific set of test conditions often are determined to be the nominal worst case based on characterization tests.

8.2.1 *Low Dose Requirements*—Hardness testing of MOS and bipolar microelectronic devices is not necessary when the required hardness is 100 rd(SiO_2) or lower.

8.2.2 *MOS Devices and Integrated Circuits with Intended Use at Dose Rates At or Below 300 rd(SiO_2)/s*:

8.2.2.1 Parties to the test must first establish the conditions of the test. These conditions should be stated in a detailed specification or other procurement document. As a minimum, the following conditions should be specified: test approach, test type, irradiation source, total dose levels, dose rate, irradiation bias, irradiation temperature, anneal bias, anneal temperature, and anneal times. The recommended default irradiation conditions are step stress, remote characterization, ^{60}Co, four dose levels (0.1X, 0.2X, 0.5X, and 1.0X, where X is the system specification), 50 to 300 rd(SiO_2)/s, static dc bias, and 24±6°C. All possible interferences of Section 6 must be considered. The two-part test given below is based on that of MIL-STD-883, Test Method 1019; however, the procedure given here does depart from Test Method 1019 where that document is considered to be too conservative.

8.2.2.2 *Test 1*—for failures related to oxide trapped charge.

(*a*) Prepare bias fixtures, test fixtures, test circuits (or test equipment), and test programs.

(*b*) Follow 8.1.1.3-8.1.1.5 as described above with the following exceptions. The time between the end of irradiation and the end of the electrical tests shall not exceed 1 h, and the time between irradiations shall not exceed 2 h.

NOTE 11—There are significant categories of semiconductor devices that show less ionizing dose damage at low dose rates than at 300 rd(SiO_2)/s. These are devices wherein the damage mechanism is dominated by build up of holes in the oxide layer, and that are only slightly affected by the build up of interface states. For low dose rates typical of space applications, the effect can be very significant. Devices, which fail at a dose level, D_f, at 300 rd(SiO_2)/s may survive at dose levels from $2D_f$ to $5D_f$ when tested at low dose rates, for example, 0.01 rd(SiO_2)/s. In some cases, characterization of these devices can permit the use of key components, which would be rejected considering only the test data taken at 300 rd(SiO_2)/s. In many other cases, it can reduce the amount of either local shielding or box shielding required to insure survivability. The methods described in 8.2.2.2 (*c*) may provide a cost effective method to make allowance for these effects.

(*c*) If the intended use dose rate is below 0.1 rd(SiO_2)/s and the parts fail at a higher dose rate, then one may perform a post irradiation room temperature anneal for a time not to exceed the specification dose divided by the maximum intended use dose rate. The anneal bias shall be the same as the irradiation bias. At the end of the anneal period remeasure the electrical characteristics and use these data to determine acceptance/rejection.

8.2.2.3 *Test 2*—For failures related to interface traps.

(*a*) An accelerated annealing (rebound) test shall be performed for failures related to interface traps, unless Test 1 is performed at the intended use dose rate or below or the conditions of 8.2.2.3 (*f*) apply.

(*b*) Prepare bias fixtures, test fixtures, test circuits (or test equipment), and test programs.

(*c*) Follow 8.1.1.3-8.1.1.5 as just described with the following exceptions. The parts shall be given an additional irradiation to raise their total dose level to 1.5 times the specification level. The time between the end of irradiation and the end of the electrical tests shall not exceed 1 h. The samples used for this test may be the same samples used for the original test.

(*d*) Following irradiation the parts shall be subjected to an accelerated anneal. Within 1 h following post irradiation electrical characterization, place the parts in an environmental chamber under the same bias used for irradiation and heat the parts to 100±5°C for 168±12 h, or for the temperature and time required by the specification. Reduce the temperature rapidly to room temperature and within 1 h following the anneal, perform the required electrical characterization to determine acceptance/rejection.

(*e*) As an alternative to 100±5°C for 168±12 h, the temperature and time may be determined by either characterization of the actual part type, or by characterization of *n*MOS transistors representative of the parts under test. If transistors are used the alternate temperature and time must demonstrate > 60 % trapped charge annealing and < 10 % interface trap annealing.

(*f*) The accelerated annealing test may be eliminated for certain part types or processes, or both, if it can be shown by characterization testing that rebound failures are not a problem for the irradiation conditions of interest. Also, it is permissible to omit the 50 % overtest requirement if characterization testing can demonstrate that the safety factor is not necessary. See Appendix X1 for a discussion of the conditions for eliminating the rebound test or the overtest requirement.

8.2.2.4 A chart summarizing the test decision flow specified in 8.2.2 through 8.2.2.3 (*f*) is given in Fig. 1.

8.2.3 *Bipolar Devices and Integrated Circuits with Intended Use at Dose Rates at or Below 300 rd(SiO_2)/s*:

8.2.3.1 The bipolar devices and circuits are divided into two categories, Category A Parts, which exhibit no dose rate sensitivity, and Category B Parts, which show enhanced degradation at lower dose rates, as described in 8.1.2.2.

8.2.3.2 *Category A Parts*—Category A Parts include all parts that have passed the screen described in 8.1.2.2 or have been determined to be dose rate insensitive by previous testing or analysis. For these parts a standard room temperature test (see 8.1.1.1-8.1.1.5 or MIL-STD-883, Test Method 1019) is sufficient for lower dose rate applications. The dose rate for these tests shall be the standard dose rate of 50–300 rd(SiO_2)/s (see 8.1.1.1 (*b*) (*1*) or MIL-STD-883, Test Method 1019) unless otherwise required by the test plan.

(*a*) Prepare bias fixtures, test fixtures, test circuits (or test equipment), and test programs.

(*b*) Follow 8.1.1.3-8.1.1.5 with the following exceptions. The time between the end of irradiation and the end of the electrical tests shall not exceed 1 h, and the time between irradiations shall not exceed 2 h.

8.2.3.3 *Category B Parts*—For parts, which are low dose rate sensitive, there are three options.

(*a*) *Option 1*—Test the parts at the average intended use dose rate if the irradiation time at the specification dose is reasonable (see Appendix X2 for discussion). This option may be

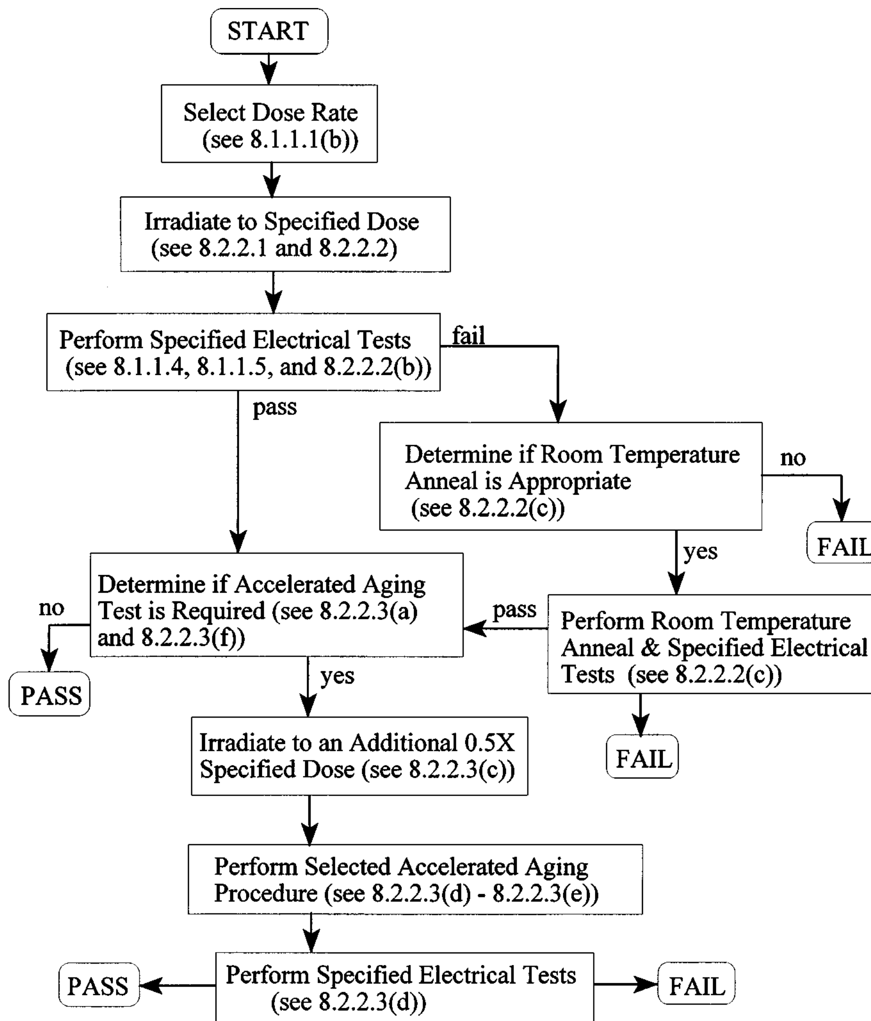


FIG. 1 Flow Chart for Ionizing Radiation Testing of MOS Devices (see 8.2.2 through 8.2.2.3 (*f*))

practical for many applications where the dose rate is no lower than 0.01 to 0.1 rd(SiO_2)/s. Follow 8.1.1.3-8.1.1.5 using the specific test conditions required by the test plan and the following exception. The time between the end of irradiation and the end of the electrical tests shall not exceed 1 h and the time between irradiations shall not exceed 2 h.

(*b*) *Option 2:*

(*1*) For some parts, irradiation at the dose and dose rate of the intended use is impractical because the resulting testing times are excessive. For such cases, an accelerated test method may be possible.

(*2*) An appropriate set of accelerated test conditions, if available, must be determined using characterization testing described in 8.1.2.4. Potential methods for achieving an accelerated test include (*a*) a high-dose-rate irradiation (50 to 300 rd(SiO_2)/s) at an elevated temperature, (*b*) a moderately low-dose-rate irradiation (0.1 to 1 rd(SiO_2)/s) at an elevated temperature, (*c*) use of an overtest, and (*d*) use of a room temperature anneal following irradiation. See Appendix X2 for discussion of these and other strategies for obtaining an accelerated test.

(*3*) The test plan for the determination of an appropriate accelerated test should receive careful attention in order to minimize cost and time. Existing data on similar devices should be used where possible.

(*4*) For such a test a well documented test procedure will be required. Follow 8.1.1.3-8.1.1.6 and 8.1.2.4 (*a*) using the specific test conditions required by the test plan and the following exception. The time between the end of irradiation and the end of the electrical tests shall not exceed 1 h and the time between irradiations shall not exceed 2 h.

(*c*) *Option 3:*

(*1*) An alternative approach may be taken, if agreed upon between the parties to the test that entails a greater level of risk than does Option 1 (see 8.2.3.3 (*a*)) or Option 2 (see 8.2.3.3 (*b*)).

(*2*) For this option, the radiation hardness assurance lot acceptance test applied to each date code shall consist of one of the following two tests: a room temperature low dose rate test at 10 mrd(SiO_2)/s, or an elevated temperature test at 10 rd(SiO_2)/s and 100±5°C. The total dose induced change in each of the sensitive parameters should be determined at the specification dose for each test.

(*3*) If the low-dose-rate test is chosen, a design margin of two should be applied. If the elevated temperature test is chosen, a design margin of three should be applied.

(*4*) Device parametric values shall be compared to the specification requirement for the parameter to determine pass or fail for the lot.

(*5*) For further discussion of the conditions specified in Option 3, see Appendix X2.

8.2.3.4 A chart summarizing the test decision flow specified in 8.2.3.2 through 8.2.3.3 (*c*) (*4*) is given in Fig. 2.

9. Report

9.1 Report the following information:

9.1.1 *Identity of the Part(s) Tested*—All information available for part identification should be included, for example, part type, serial number, manufacturer, lot date code, diffusion lot designation, wafer lot designation, package type, etc.

9.1.2 The test plan containing a listing of items agreed upon by parties to the test including all conditions of 4.1.2.2, for example, nature and spectrum of the radiation source, dose rates, time sequences, and dosimetry techniques and measurements.

9.1.3 A schematic for the bias and parameter measurement circuits.

9.1.4 A diagram of the physical test configuration with distance and materials.

9.1.5 A tabulation of test parameter measurement data including electrical noise and current leakage of the electrical measurement system for in-flux testing, the test date, the radiation source used, the bias conditions during irradiation and transport, the ambient temperature around the device

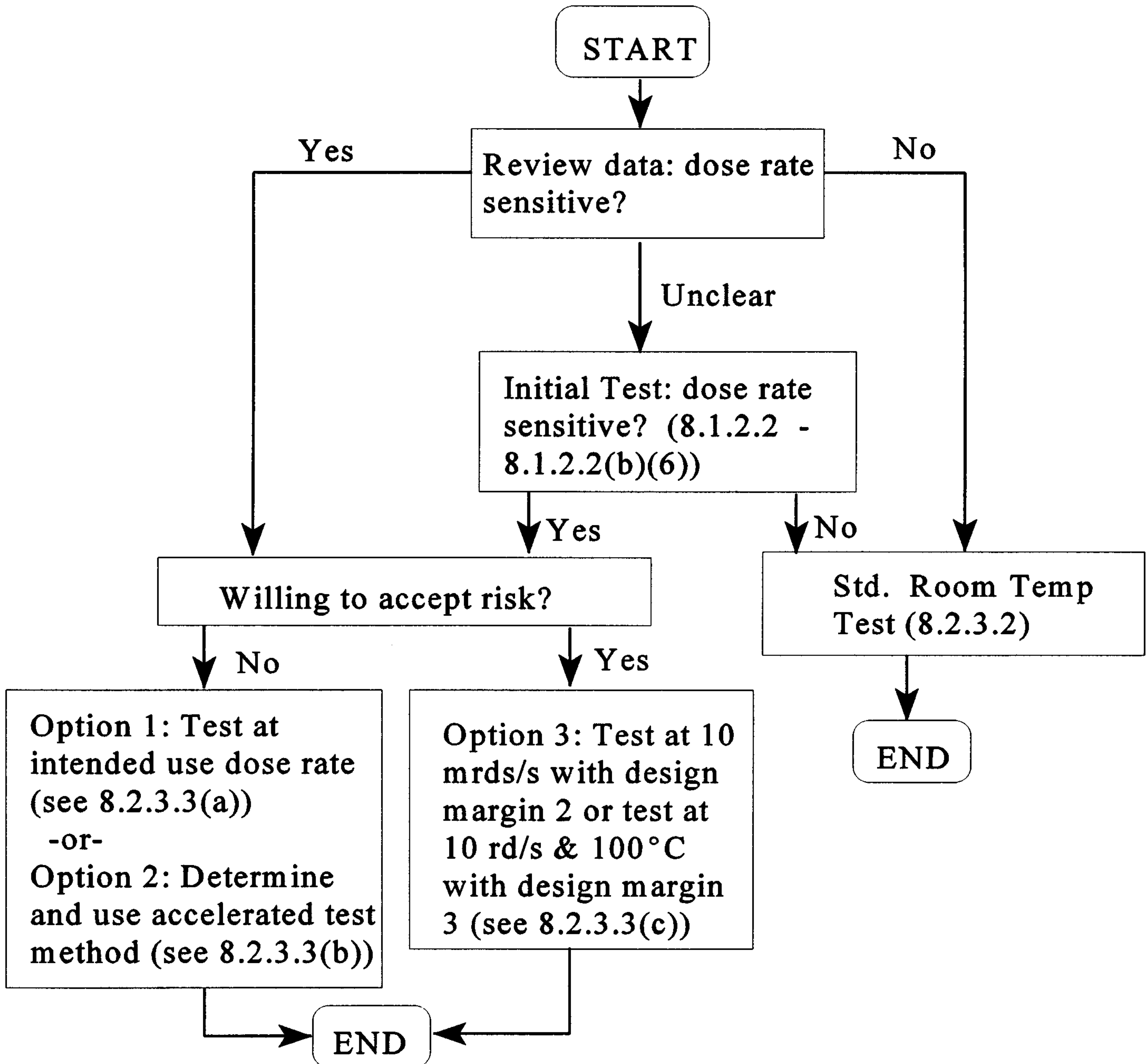


FIG. 2 Flow Chart for Lot Acceptance Testing for Bipolar Devices (see 8.2.3 through 8.2.3.3 3 (*c*) (*4*))

during irradiation and testing, the duration of each irradiation, the time between irradiation and electrical testing, the duration of the electrical measurements, the time to the next irradiation, the electrical test conditions and the radiation test (dose) levels;

9.1.6 Any anomalous incidents during the test.

9.1.7 A description of the accelerated annealing procedure, if used.

9.1.8 For bipolar devices, whether Category A or Category B, test conditions used if Category B, and how those test conditions were established.

9.1.9 For procurement testing the pre- and post-irradiation data shall be recorded for each part and retained with the parent population data.

10. Keywords

10.1 ASIC (application specific integrated circuit); bipolar; cobalt 60 testing; gamma ray tests; ionizing radiation testing; MOS; radiation hardness; semiconductor devices; time dependent effects; total dose testing; X-ray testing

APPENDIXES

(Nonmandatory Information)

X1. MOS (METAL OXIDE SEMICONDUCTOR) DEVICES AND CIRCUITS

X1.1 *Scope*—Because of their low power requirements and increasing dominance in the digital IC world, MOS electronics are very important components of virtually all military and space systems. Most of the discussions in this appendix describe total-dose qualification of parts for space and other low-dose-rate radiation environments. A detailed discussion of the technical basis for the MOS test method in 8.2.2 is provided, and alternative test methods are discussed. A brief discussion of tactical and higher-dose-rate weapon environments also is included. Examples are limited to small-signal electronics, but discussions also generally apply to power MOS.

X1.2 *Background*—MOS total-dose response is governed almost exclusively by ionization effects in critical insulating layers in the devices, most notably gate and field oxides, and by defect buildup at or near the critical interface between the silicon channel layer and the SiO_2 gate oxide **(1-3)**.[7] A schematic illustration of the most important defects in modern MOS gate oxides **(4)** is shown in Fig. X1.1. Defect location is shown in Fig. X1.1(*a*), and impact on electrical response is indicated in Fig. X1.1(*b*). Historically, defects in the MOS system have been grouped into "oxide traps" and "interface traps." For thermal oxides in a radiation environment, the dominant oxide-trap charge is positive and due primarily to radiation-induced trapped holes. These shift the threshold voltage of a MOS transistor negatively. Interface traps shift the threshold voltage of an *n*-channel MOS transistor positively, and that of a *p*-channel transistor negatively **(1-4)**. Interface traps also lead to mobility degradation **(5,6)**. Recently, it has become clear that it can be difficult with standard characterization techniques to distinguish the effects of interface traps and near-interfacial oxide traps, that is, border traps, on MOS transistor I-V characteristics **(4)**. Although this can be an important distinction in studies of MOS radiation physics, presently it is not thought to be critical to discussions of MOS hardness assurance. The historical convention, therefore, will

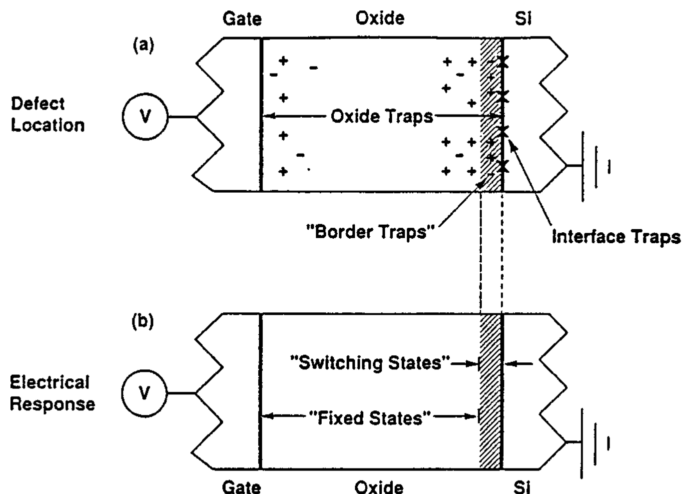
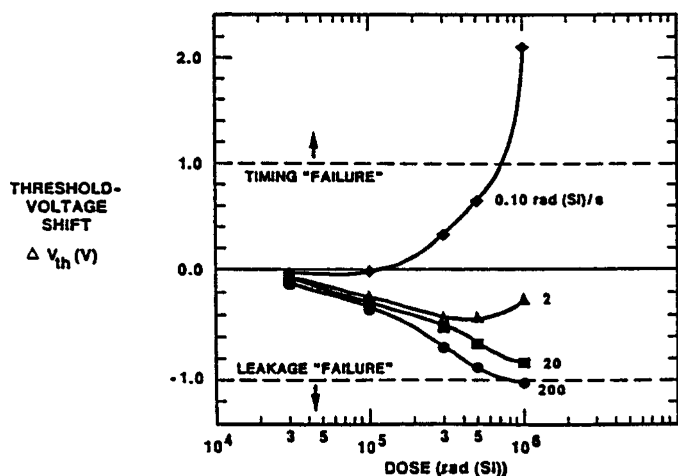


FIG. X1.1 Physical Location (*a*) and Electrical Response (b) Associated With Defects in MOS Gate Oxides (Ref 4)

be adopted of assuming that most defects that do not exchange charge with the silicon during the measurements ("fixed states" in Fig. X1.1(*b*)) are oxide traps, and most defects that exchange charge with the silicon ("switching states" in Fig. X1.1(*b*)) are interface traps.

X1.2.1 *Dose-Rate Effects on MOS Total-Dose Response*—Fig. 2 shows threshold voltage shifts as a function of dose rate for an early Si-gate radiation-hardened CMOS process **(7)**. Irradiations at dose rates typical of conventional laboratory sources (20 to 200 rd(SiO_2)/s) show relatively large negative threshold voltage shifts at a dose of 1 Mrd(SiO_2). A negative threshold voltage shift in an *n*MOS transistor can cause failures due to excess leakage current in MOS IC's. Testing at lower dose rates, however, closer to space environments, shows large positive threshold voltage shifts in Fig. X1.2 at lower total doses. Positive threshold voltage shifts, often called "rebound" or "super-recovery," in which the value of the threshold voltage not only "turns around" with increasing total dose, but also exceeds its preirradiation value **(8,9)** can lead to circuit and system failures due to reductions in noise margin, speed, and timing problems **(7,10)**. Testing some types of MOS devices at

[7] The boldface numbers in parentheses refer to the list of references at the end of this standard.

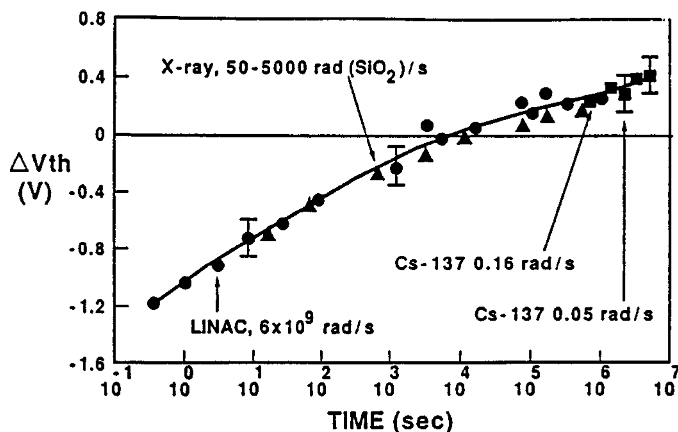


NOTE 1—The "failure levels" indicated on the figure at ± 1 V are for illustration purposes only. Real failure doses in MOS IC's may be at higher or lower levels (**Ref 7**).

FIG. X1.2 Threshold Voltage Shifts Versus Dose and Dose Rate for ^{60}Co (2 – 200 rd(SiO_2)/s) and ^{137}Cs (0.1 rd(SiO_2)/s) Irradiations of MOS Transistors With 45-nm Thick Gate Oxides

rates of 20 to 200 rd(SiO_2)/s, therefore, can give both the wrong failure dose and the wrong failure mode for a lower-dose-rate space application.

X1.2.2 *Technical Basis for MOS Hardness Assurance Tests*—Fig. X1.3 shows threshold voltage shifts as a function of postirradiation anneal time for *n*MOS transistors with 60-nm gate oxides. "Zero" on the time axis is taken to be the beginning of each of the respective irradiation periods. Data are shown for LINAC, X-ray, and ^{137}Cs irradiations to a total dose of 100 krd(SiO_2) at 6 V bias, followed by room-temperature anneal at the same bias. Dose rates range from 6×10^9 to 0.05 rd(SiO_2)/s. At high rates, the threshold-voltage shifts are fairly large and negative, dominated by oxide-trap charge. At lower rates, the shifts are positive, indicating an excess of interface traps. Threshold-voltage shifts following high-rate irradiation plus room-temperature anneal at the same bias are equal, to within experimental uncertainty, to low-dose-rate exposures at equivalent times. Similar trends are observed for the growth of interface trap charge and the annealing of oxide-trap charge (**11**). The response of MOS devices under these irradiation and anneal conditions, thus, falls on universal defect growth and annealing curves over an extremely wide range of dose rates (**11-15**). That is, fundamentally different processes are not occurring during irradiation at different dose rates; the apparent dose rate effects are due to differences in time dependent oxide-trap charge neutralization and interface-trap buildup. The equivalence of high-rate irradiation and annealing to low-rate response occurs only when electric fields and temperature are constant throughout the irradiation and annealing sequences (**11**). This does not present a practical problem for MOS devices under typical worst-case radiation response conditions, but causes difficulties in defining hardness assurance tests for bipolar devices, as discussed in Appendix X2.



NOTE 1—The irradiation and anneal bias was 6 V (**Ref 11**).

FIG. X1.3 Threshold Voltage Shifts for nMOS Transistors With 60-nm Gate Oxides Versus Postirradiation Anneal Time For Varying Dose Rate Exposures to a Dose of 100 krd(SiO_2)

X1.3 *Low-Dose-Rate Hardness Assurance*

X1.3.1 It must be recognized that one cannot perform a cost-effective standard test that fully simulates the response of a MOS device at the end of its life in a space environment. This is because with higher-rate irradiations or anneals, or both, one cannot reproduce simultaneously the amount of oxide- and interface-trap charge that will exist in an irradiated MOS oxide after years of exposure in space. Instead, one can only define a test sequence that will ensure that a device will perform within consistent, bounded limits during its lifetime. The method in 8.2.2 was developed subject to the following general constraints (**12-16**):

X1.3.1.1 The test must screen out both interface- and oxide-charge related failures.

X1.3.1.2 The test must work for both hardened and commercial ICs.

X1.3.1.3 The test must be conservative, that is, some good product is allowed to be excluded on the basis of the test method, but bad product is not allowed to be accepted.

X1.3.1.4 The test must be relatively inexpensive, and easy to perform and interpret.

X1.3.1.5 The test must not depend on the availability of test structures. Indeed, the method should be useful even in absence of pre-existing knowledge about an ICs radiation response.

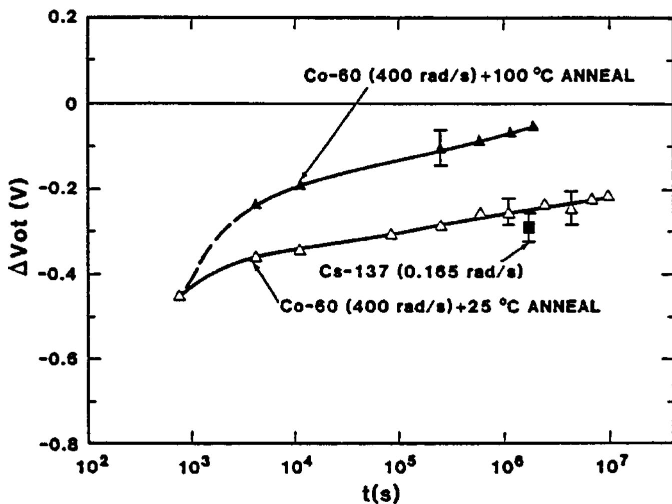
X1.3.1.6 Because of these constraints on a standard test method, optimized tests can be developed for a well-characterized technology that improve on standard tests, for example, by being less conservative, as illustrated below. In general, the tests outlined below have been shown by experience to be conservative for MOS technologies.

X1.3.2 *Test Requirement*—Because oxide traps shift the threshold voltage negatively, and interface traps shift the threshold voltage for an *n*MOS transistor positively, at least a two-step test must be performed to assess the suitability of MOS devices or ICs in a low-dose-rate environment in a practical, cost-effective manner, unless either oxide trap or interface trap effects can be rigorously demonstrated to be negligible in a technology of interest.

X1.3.2.1 *Bounding Oxide-Trap Charge Effects*—Oxide-trap charge decreases monotonically with decreasing dose rate or

annealing time (**7-11**). As long as the dose rate of any laboratory exposure is greater than the expected dose rate in space, there will be more oxide-trap charge after the laboratory irradiation than in space. Further, because interface-trap charge tends to increase with increasing irradiation or annealing time, or both, there will be less interface-trap charge after a laboratory exposure than in space. Together, these two points ensure that gate, or field, oxide transistor threshold voltage shifts will be more negative after laboratory exposure described in 8.2.2.2 than in space (see Fig. X1.3), so a laboratory test is already conservative with respect to oxide-trap charge effects (**11-16**). Bounding interface trap effects in space is more difficult. With room temperature irradiation or room-temperature annealing, or both, one can never be sure that one has performed a fully conservative test for positive threshold voltage shifts and mobility degradation effects associated with interface traps. This is because there will always be more oxide-trap charge and fewer interface traps following such a sequence than in space. See Fig. X1.3, for example. With increasing irradiation or anneal time, or both, the *n*MOS threshold voltage shift is becoming more and more positive. Attempts to "simulate" MOS response in space simply by performing a low-dose-rate irradiation (at a rate that does not closely approximate the actual rate experienced in the application), therefore, are inherently nonconservative, unless characterization tests have been performed to show that no further interface-trap growth or oxide-trap charge annealing occur in the devices of interest on time scales longer than that of the exposure.

X1.3.2.2 *Bounding Interface-Trap Charge Effects*—To provide a conservative test for interface-trap effects in space, one must ensure that the second part of the test sequence (8.2.2.3) leads to a more positive *n*MOS threshold voltage shift following the laboratory test than will occur in space (**13-15**). Figs. X1.4-X1.6 show how "rebound" testing accomplishes this goal. First note in Figs. X1.4-X1.6 that ^{60}Co irradiation to 300 krd(SiO_2) at a dose rate of ~400 rd(SiO_2)/s followed by ~ 10^6 s of room-temperature annealing at the same bias (6 V) is equivalent to a 0.165 rd(SiO_2)/s ^{137}Cs exposure. In Fig. X1.4, the net oxide-trap charge recovery is accelerated by raising the temperature during annealing to 100°C (**9**), and in Fig. X1.5 the interface-trap buildup rate increases with 100°C annealing. This combination is ideal for providing a conservative test of interface traps at low dose rates; the oxide trap charge is minimized, and the interface-trap charge is maximized. Both components therefore, act to make the threshold shift more positive during annealing, as shown in Fig. X1.6. More importantly, the value of the threshold voltage shift in Fig. X1.6 is significantly more positive after the annealing sequence than it would be after a much longer period at 25°C, given any kind of reasonable extrapolation of the threshold-voltage shift during the next 1 to 2 decades of time in the 25°C data of Fig. X1.6.



NOTE 1—Gates were biased at 6 V during irradiation and annealing. Anneal temperatures were 25°C or 100°C (**Ref 15**).

FIG. X1.4 Threshold Voltage Shift Due to Oxide-Trap Charge for nMOS Transistors With 32-nm Oxides, Irradiated to 300 krd(SiO_2) With ^{60}Co or ^{137}Cs Gamma Rays

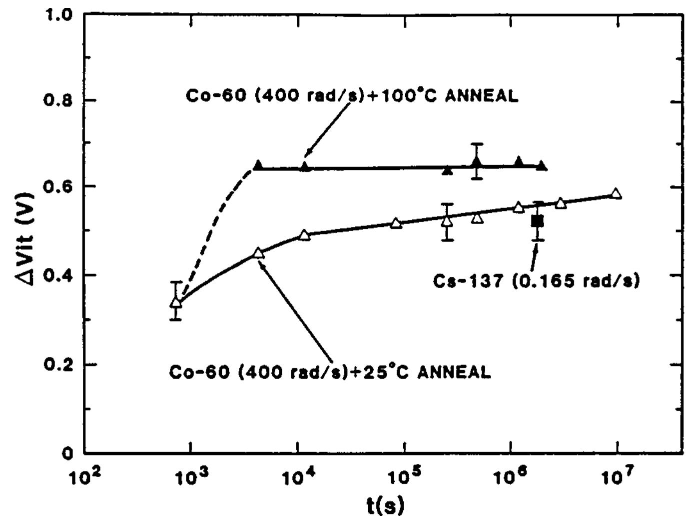


FIG. X1.5 Threshold Voltage Shifts Due to Interface Traps for the Devices of Fig. X1.4 (Ref 15)

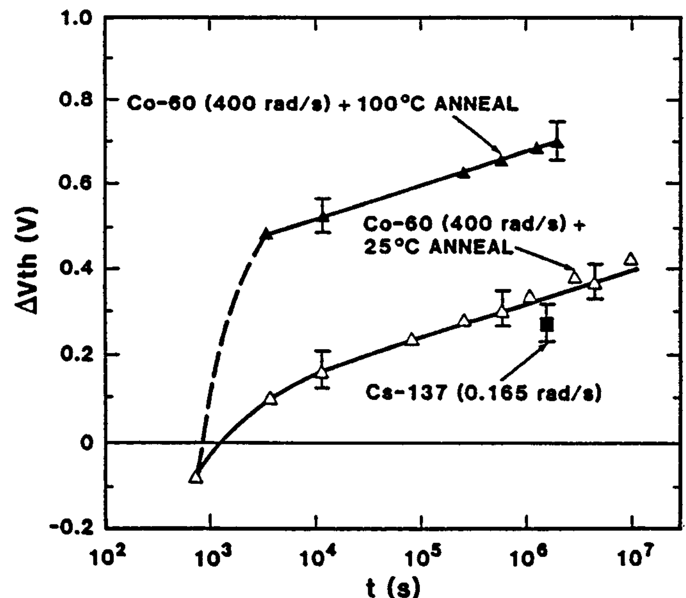


FIG. X1.6 Net Threshold Voltage Shifts for the Devices of Fig. X1.4 and Fig. X1.5 (Ref 15)

X1.3.2.3 *Accelerated Annealing Test*—Figs. X1.4-X1.6 and other experience with MOS devices **(11-16)** suggest that a "rebound test" at 100°C is a suitable accelerated annealing test for interface-trap effects at low dose rates. An additional irradiation is specified in 8.2.2.3, Test 2, (*c*) to account for uncertainties in determining worst-case bias during irradiation and anneal, and to account for the possibility of *p*MOS threshold voltage recovery during the anneal **(13,15,17)**. Paragraph 8.2.2.3 allows some latitude in choosing the details of the accelerated annealing test, based on characterization test results. Care must be exercised that significant interface-trap annealing, however, does not occur at the temperature chosen for the rebound test, which becomes an increasing risk above 100°C **(15)**.

X1.3.2.4 *Omitting the Accelerated Annealing Test*—Accelerated annealing tests are necessary for many part types, and their expense can be a small price to pay to avoid catastrophic system failure due to improper part selection. Nevertheless, it is more expensive to do rebound testing than it would be to omit it, if safe to do so. For this reason, 8.2.2.3 contains many ways to avoid rebound testing as part of a routine lot acceptance program. An obvious case where an accelerated annealing test is not needed is an application in which the duration of the possible radiation exposure in the environment of interest is comparable to the Co-60 irradiation time in 8.1.1. For cases in which parts must survive for long times after irradiation exposure, or during low-dose-rate exposures, one must consider other ways in which accelerated annealing tests may be omitted. One way is to perform full characterization tests on devices made in the same process technology. If it can be demonstrated that rebound failures are not a problem for the devices and irradiation conditions of interest, 8.2.2.3 allows the rebound test to be omitted during lot acceptance. This action should not be taken lightly, and certainly not without evidence that the devices are being manufactured on a process line for which variables that affect radiation-induced interface-trap buildup, like postoxidation temperatures and annealing ambients **(1,18)**, are under careful control. Evidence of sufficient control could be demonstrated, for example, with lot sample tests using a 10-keV X-ray source to irradiate test structures that accompany product wafers **(18)**. If, and only if, (*1*) interface-trap densities of test structures remain under statistical process control, and (*2*) their level is below trap densities for which it has been demonstrated that product circuits will pass testing for the given application, including rebound testing, then it is reasonable for the parties to the test to agree to waive rebound testing during routine lot acceptance of product from that line to avoid unnecessary expense.

X1.3.2.5 *Accelerated Annealing Test Issues for Commercial Parts*—Unfortunately, not all product required for low-dose space systems can be procured from vendors who can (or will) demonstrate sufficient control of interface-trap densities to allow a waiver on rebound testing. Certainly, this would almost never be the case for a commercial line in which radiation hardness is neither a requirement nor a consideration during the product cycle **(19)**. For a commercial line, a successful "spot test" on one product run cannot be used to "bless" future (or past) product runs, without evidence of control of variables impacting radiation hardness, which is virtually impossible to obtain from a purely commercial line. For low-dose systems, however, it may be possible to waive rebound testing on the basis of a first-principles estimate of the maximum number of interface traps that can be generated in a MOS transistor with a gate oxide of a given (known) thickness. In Fig. X1.7, the maximum positive threshold voltage shift is plotted that interface traps may induce in MOS devices with 20-nm, 50-nm, and 100-nm oxides **(13,20)**. Specifically, interface-trap buildup is described in the following equation:

$$\Delta V_{it} \approx (q/\epsilon_{ox})\, \kappa_g\, f_y\, f_{it}\, (t_{ox})^2\, D \quad \text{(X1.1)}$$

where:

$-q$ is the electronic charge,
ϵ_{ox} is the oxide dielectric constant,
κ_g (the charge generation efficiency) is the number of electron-hole (e-h) pairs generated in SiO_2,
f_y is the probability that a given e-h pair does not recombine,
f_{it} is the interface-trap generation efficiency, that is, the total number of interface traps eventually created per e-h pair,
t_{ox} is the thickness of the SiO_2 gate oxide, and
D is the dose.

The values of Fig. X1.7 were calculated assuming a charge generation efficiency of ~ 8 × 10^{12} $cm^{-3}rd^{-1}(SiO_2)$, and a charge yield of ~ 80 % **(13)**, both of which are reasonable for biased MOS devices in space. A value of f_{it} of ~ 20 % was selected as typical of, or greater than, values of f_{it} or MOS devices that exhibit very large interface-trap buildup **(13)**. Shifts in Fig. X1.7 assume no offsetting contribution to threshold voltage due to oxide-trap charge, even though this will be non-zero in space, and thus, provide an approximate upper bound on the maximum device rebound for a given gate oxide thickness. Interface traps in field oxide regions of MOS devices do not adversely affect device response because they shift the field oxide threshold voltage away from depletion, so only interface traps in the gate oxide need be considered in this estimate. Except for circuits with delicate timing requirements or low noise margin, or devices like power MOSFETs where it may not be possible to tolerate even small reductions in output drive current, circuits and devices with gate oxides thinner than ~ 100 nm often can function with the small positive threshold-voltage shifts observed below 5 krd(SiO_2) (dashed line) in Fig. X1.7. For thinner oxides, this point of automatic acceptability moves to higher doses. For example, Eq X1.1 suggests that a

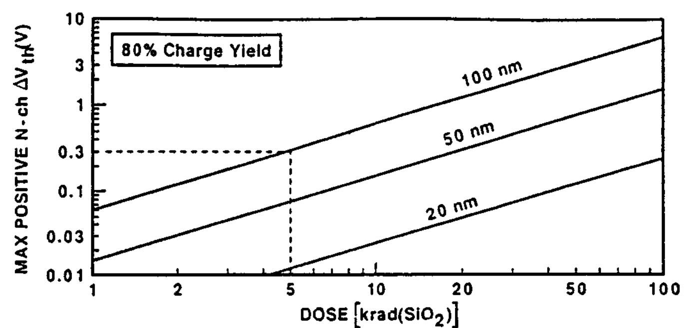


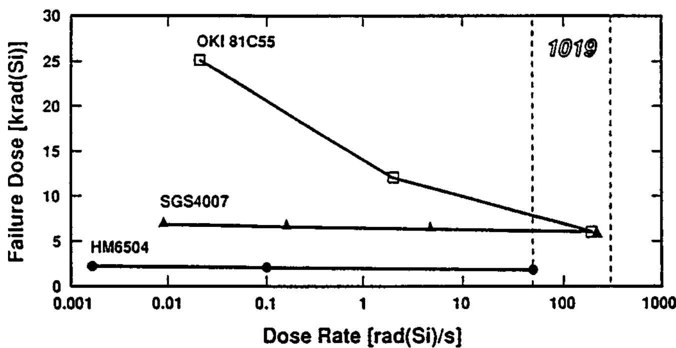
FIG. X1.7 Maximum Positive Threshold Voltage Shift as a Function of Dose for nMOS Transistors, Calculated Under the Conditions of Eq. 1(Refs 13,20)

10-nm oxide should have less than about +0.06 V rebound at 100 krd(SiO_2). For thin enough gate oxides and low enough total dose requirements, it should be possible to waive rebound testing in many cases **(13,16,20)**. Of course, in absence of knowledge about device processing or circuit response, a limited amount of characterization testing that includes elevated-temperature annealing to screen for possible interface-trap effects certainly would be prudent for sensitive devices and ICs.

X1.3.2.6 *Less Conservative Oxide-Trap Charge Tests*—A less conservative test than Condition A, 8.1.1.1 (*b*) (*1*) is useful for low-dose space systems, for example, 5 to 20 krd(SiO_2)), for which some commercial non-radiation-hardened devices might fill system needs. For example, Fig. X1.8 illustrates how the failure dose of three commercial devices depends on the dose rate of the exposure. The Oki 81C55 is a device with a rapidly-recovering field oxide that causes failure during ^{60}Co irradiation at 50–300 rd(SiO_2)/s, but not at dose rates (< 0.1 rd(SiO_2)/s) typical of space applications **(7,10)**. At low rates, failure is caused by oxide charge trapping in the MOS gate oxide **(7)**. The SGS 4007 and the Harris HM6504 are commercial devices that recover very slowly after ^{60}Co irradiation at 50 to 300 rd(SiO_2)/s, and exhibit failure doses at low dose rates that are similar to those observed at high rates **(13)**. The Oki device, then, is typical of devices that will function at much higher doses in space than during ^{60}Co exposure at 50 to 300 rd(SiO_2)/s, and the HM6504 and SGS 4007 are typical of slow-annealing devices that will fail in space at doses only slightly higher than during ^{60}Co exposure at 50 to 300 rd(SiO_2)/s.

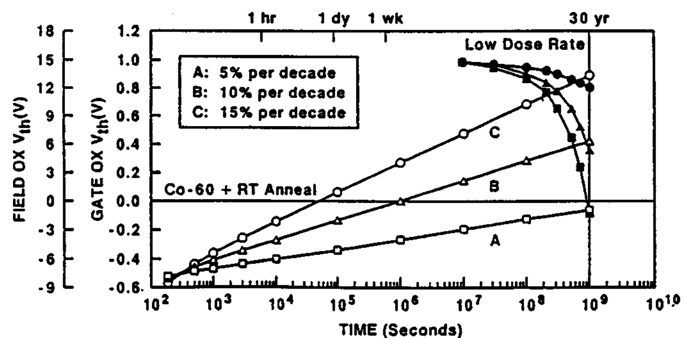
X1.3.2.7 *Lower Dose Rate Irradiation*—One type of less conservative test for oxide-trap charge failure in space is simply to irradiate at lower dose rates. This is illustrated by the Oki data of Fig. X1.8. Lower-dose-rate irradiation leads to a higher dose-to-failure than ^{60}Co irradiation at 50 to 300 rd(SiO_2)/s, but still provides a conservative test for oxide charge effects at the still lower dose rates (<< 0.01 rd(SiO_2)/s) typical of many space systems. This is equivalent to using Condition C in 8.1.1.1 (*b*) (*3*). There are some practical difficulties with this approach. Low-dose-rate exposures often are expensive, difficult, and time consuming. There also are challenges associated with dosimetry at very low dose rates **(11)**. Moreover, for devices like the HM6504 and the SGS 4007 in Fig. X1.8, one could perform very-long-term exposures and still find that the device is unsuitable for system application. These potential difficulties do not rule out low-dose-rate irradiation as a less conservative test of oxide-trap-charge related effects in space, especially for systems with modest total dose requirements that allow low-rate exposures to be performed on manageable time scales.

X1.3.2.8 *Irradiation Plus Room Temperature Anneal*—An alternative to low-dose-rate testing is irradiation plus room temperature anneal. In Fig. X1.9 the response of non-radiation-hardened oxides has been simulated after ^{60}Co irradiation and 25°C anneal via linear response theory **(13)**. The approach taken to derive these results has been validated for many types of MOS circuits and devices **(11-16)**. In Fig. X1.9 the response of MOS devices following ^{60}Co irradiation and room-temperature anneal is compared to their projected response after low-dose-rate irradiation to the same dose. Interface trap effects are neglected here and would have to be assessed separately via rebound testing at the conclusion of the room temperature anneal. To generalize the discussion to higher and lower annealing rates, simulated irradiation and anneal curves are plotted in Fig. X1.9 for otherwise identical devices having annealing rates of 5 and 15 % per decade of annealing time (Curves A and C, respectively). Here, failure is defined to be the point at which the *n*MOS gate- or field-oxide threshold voltage becomes less than 0 V; that is, the point at which the gate or parasitic field oxide transistor goes into depletion mode. At or near this point, increased leakage in the device can lead directly to circuit functional failure or to system failure because of excessive power dissipation. Fig. X1.9 shows that devices with gate or field oxides that trap large amounts of oxide charge and anneal very slowly (Curve A) fail after ^{60}Co irradiation (V_{th} < 0 *V*), and also fail in space for the same reason. Faster annealing devices (Curves B and C) also fail after ^{60}Co irradiation (V_{th} < 0 *V*), but function acceptably at



NOTE 1—Irradiations at dose rates greater than 1 rd(Si)/s were performed with Shepherd or AECL gamma sources. Irradiations at lower rates were performed with Shepherd ^{137}Cs sources. For these sources, dose (Si) ≈ dose (SiO_2) **(Ref 13)**.

FIG. X1.8 Failure Dose Versus Dose Rate for Three Types of Commercial MOS Devices



NOTE 1—Data points are derived from linear response analysis predictions, which are variations on a set of experimental annealing data, as described in Ref. **(Ref 13)**. The starting value of the threshold voltage is taken to be 1 V for the gate oxide and 15 V for the field oxide. No significant changes occur for times less than 10^7 s for the low-rate response curves.

FIG. X1.9 Projected Values of nMOS Gate-Oxide or Parasitic Field Oxide Threshold Voltage for Non-Radiation-Hardened MOS Transistors

low dose rates ($V_{th} > 0$ V; solid symbols, low-rate curves). The devices of Curve C recover ($V_{th} > 0$ V) approximately one day after higher-rate irradiation, and the devices of Curve B recover after about 11 days (~ 10^6 s). For any reasonable annealing time, however, even up to 1 year (~ 3×10^7 s), the threshold voltage is more negative following ^{60}Co irradiation and room-temperature annealing than at the end of the low-dose-rate exposure for Curve A. Fig. X1.9 and other experience with MOS devices and circuits **(16)**, therefore, confirms that ^{60}Co irradiation and room-temperature annealing can provide a conservative response of oxide-charge related failure in space, but the estimate is less conservative than that provided by Condition A of 8.1.1.1 (*b*) (*1*).

X1.3.2.9 *Limitation on Room Temperature Anneal Time*—On the basis of Fig. X1.9, one could extend the annealing period indefinitely and obtain even more realistic estimates of oxide-trap charge effects in space. One must ensure, however, that the total annealing time at room temperature, t_A, does not exceed $t_{A,max}$, where:

$$t_{A,max} = D_T/R_M \quad (X1.2)$$

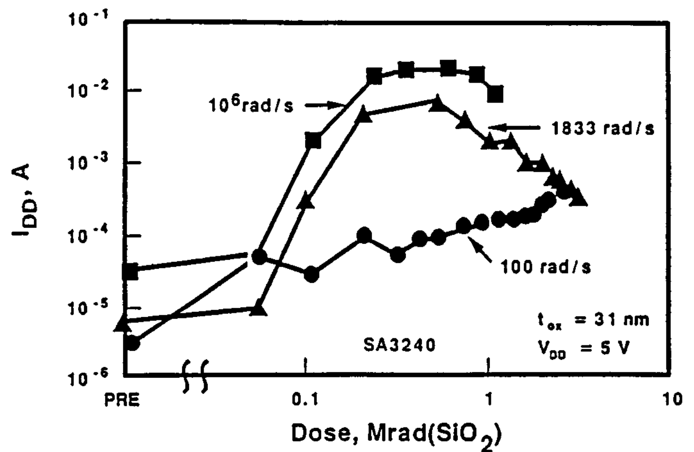
where:
D_T is the system total-dose specification, and
R_M is the maximum dose rate at which any significant dose is deposited **(14)**. The limitation on t_A is necessary for systems in which a significant fraction of the dose can be deposited during a relatively short portion of the mission, for example, during a solar flare or an excursion into the radiation belts **(21)**. This equation also is a potentially important constraint to military space systems, where a satellite not only must survive the natural radiation encountered in space, but also must survive higher-rate weapon-related radiation environments. Keeping $t_A < t_{A,max}$ prevents devices that could fail during the brief period of exposure at higher dose rates from being accepted on the basis of their longer-time recovery. For systems in which nearly all of the total dose is deposited at approximately the same rate, Eq X1.2 provides no practical limitation on the allowed annealing times. For mixed-rate systems, as long as the above limit on anneal time is observed, ^{60}Co irradiation plus room-temperature annealing can provide an estimate of the effects of oxide-trap charge on MOS response in space. Especially for commercial technologies, annealing rate is a crucial parameter to monitor during technology characterization and hardness assurance testing for low-dose-rate applications.

X1.3.2.10 *Limitation on Room Temperature Anneal Temperature*—If the leakage current induced by the initial radiation exposure becomes so large that it heats the devices significantly, the irradiation plus room temperature anneal test can become nonconservative due to thermally-assisted over-annealing of the oxide-trap charge. It is important, therefore, that the IC remains truly at room temperature during annealing and does not self-heat. Of course, the test method specifies control of the device temperature during irradiation for the same reason in 8.2.2.1, so such parts should be identified at the irradiation-testing phase.

X1.3.2.11 *Limitation on Failure Criteria*—Parts that experience functional failure during testing often become de-biased, leading to radiation-induced recovery **(16)**. For this reason, only parts with parametric failures are allowed to go into the room temperature anneal in 8.2.2.2 (*c*). Parts that fail functionally at higher dose rates due to excessive leakage must be irradiated at a low enough rate that function failure does not occur, subject to the constraints of 8.1.1.1 (*b*) (*3*) Condition C, if one wishes to pursue lot acceptance of such devices.

X1.4 *Dose Rates Greater Than 300 rd(SiO_2)/s*—For tactical and high-dose-rate weapon applications in which the dose rate of exposure greatly exceeds 300 rd(SiO_2)/s, the test flow of Section 8 often does not provide a conservative estimate of MOS response **(22)**. One such example is shown in Fig. X1.10. Here the quiescent leakage current, I_{DD}, of a 16k Static RAM is plotted as a function of dose for three different dose rates: 10^6, 1833, and 100 rd(SiO_2)/s. At the higher rates, there is a large increase in leakage current at 100 to 200 krd(SiO_2) due to the turn-on of a parasitic edge transistor associated with the field oxide in these devices. At the lowest rate, no such increase is observed. These differences in response are due to the decrease in oxide-trap charge and increase in interface-trap charge in the edge region with decreasing dose rate, or increasing anneal time, or both, that prevents the parasitic device from turning on and increasing I_{DD} at the lowest rate. Oxide-charge related failures in high-dose-rate radiation environments are not always identified in testing in accordance with Section 8. For these environments, one must either test under conditions that simulate the environment of interest, for example, by exposing the devices at a LINAC or flash X-ray source, or a derivative test method must be employed **(16,22)**.

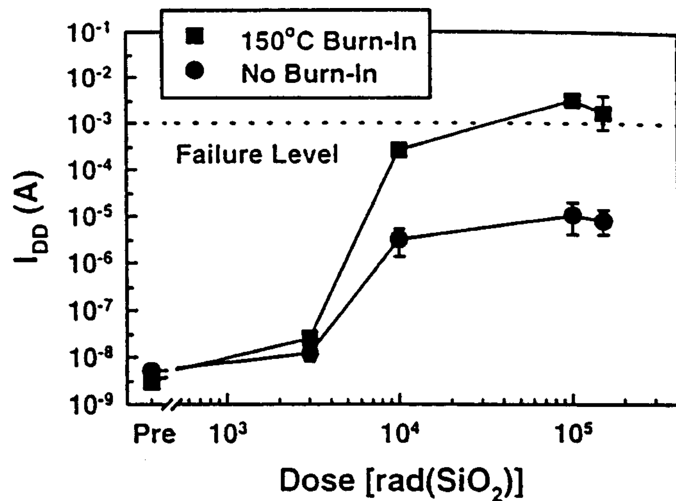
X1.4.1 *High-Dose, High-Dose-Rate Environments*—The reader is cautioned that when using some types of high-total-dose, high-dose-rate radiation environments there is no suitable alternative to testing at a suitable high-dose-rate source that can approximate the environment of interest **(16)**. Moreover, special care is required for MOS devices and ICs built in SOS/SOI (silicon on saphire, silicon on insulator) technology due to potential back-gate and sidewall leakage issues. For a detailed discussion of testing alternatives in these cases see Ref **(16)**.



NOTE 1—The 100 rd/s exposures were in a ^{60}Co source, the 1833 rd/s exposures were with 10-keV X rays, and the 10^6 rd/s tests were with 230-MeV protons at the TRIUMF cyclotron at the University of British Columbia in Vancouver, Canada. **(Ref 22)**

FIG. X1.10 Quiescent Leakage Current Versus Dose for IC's Irradiated at Rates of 100, 1833, and 10^6 rd(SiO_2)/s

X1.4.2 *10-keV X-ray Irradiation*—10-keV X-ray tests often are performed to characterize the basic radiation response of MOS structures, track the hardness of a given technology via test structure irradiations, and provide quick feedback about the hardness of a lot before submitting it to the further expense of packaging the devices and performing ^{60}Co-based lot acceptance testing (see Ref **18** and Guide F 1467). The data of Fig. X1.10 suggest that, because of the higher dose rates associated with typical 10-keV X-ray exposures (see Ref **22** and Guide F 1467), such irradiations also might be useful in a hardness assurance test plan for MOS electronics intended for use in some types of weapon applications. Issues of X-ray penetration depth, charge yield, and dose enhancement must be addressed before one can use 10-keV X-ray irradiation to qualify parts for high-rate radiation environments. A full discussion of these issues is provided in Guide F 1467. If these issues can be addressed within the framework of the testing requirements, a 10-keV X-ray source can provide assistance in lot acceptance for high-dose-rate applications **(11,16,22)**.



NOTE 1—The dashed line represents a parametric failure level of 1 mA. **(Ref 24)**

FIG. X1.11 Static Power Supply Leakage Current as a Function of Dose for Commercial Octal Buffer/Line Drivers With or Without a Pre-Irradiation 150°C Burn-In, Irradiated With ^{60}Co Gamma Rays at 90 rd(SiO_2)/s

X1.5 *Burn-In Effects*—A complication in the traditional MOS lot acceptance flow is work showing that reliability screens, for example, burn-in, normally given devices before product is shipped sometimes can affect significantly their radiation response **(23)**. Because burn-in is performed at a much lower temperature than the device has already experienced during processing, it had been presumed previously that the radiation response of burned-in and non-burned-in devices would be similar, so lot samples for radiation testing could be pulled, to save time and expense, without receiving a burn-in. Fig. X1.11 illustrates the danger of testing devices without burn-in. These commercial octal buffer/line drivers have a problem with excess leakage current in a radiation environment. In Fig. X1.11, devices, which received a burn-in, show much higher leakage currents after ^{60}Co irradiation to 150 krd(SiO_2) than do parts which did not receive a burn-in. The non-burned-in parts easily pass the parametric test limits for these devices, while burned-in parts, more representative of shipped-product response, fail the test. At higher dose rates typical of some weapon environments, these parts could cause system failure due to their high leakage currents. Failures even could occur in space systems in oxide-trap charge annealing rates that are not high enough for the devices to recover before the leakage current becomes great enough to cause circuit or system failure **(22,23)**. Enhanced leakage currents associated with burn-in also have been observed in he hardened SRAMs of Fig. X1.10 **(23)**. An initial characterization study of gate and field oxide transistors suggests that burn-in may alter some interface-trap precursors in these technologies **(24)**. Without compensating interface traps, gate-, field-, or edge-transistor leakage can be unacceptably high in high- or low-dose-rate applications **(16,22,23)**. If devices are to be burned-in before being used in such systems, the results of Ref. **(23)** show clearly that one must perform radiation testing on burned-in parts, unless the devices have been shown not to exhibit changes in radiation response due to burn-in, or unless the response of burned-in devices can be correlated accurately to that of non-burned-in devices. This effect also must be considered in interpreting the results of wafer level irradiations on non-burned-in devices for technologies that show this effect. Finally, the sensitivity of device radiation response to burn-in is most likely not unique to MOS technologies, as bipolar and BiCMOS devices, which are prone to show parasitic leakage in recessed or trench field also may be susceptible to these burn-in effects.

X2. BIPOLAR DEVICES AND CIRCUITS

X2.1 *Purpose and Organization*—This appendix supports those sections of the main document, which deal with bipolar devices and circuits. Background information and a discussion of total dose response mechanisms in discrete bipolar transistors and digital and linear microcircuits are provided. Mechanisms in the sensitive oxides, the transistors, and the circuits are addressed. Specific details to support the bipolar issues in Section 6 on interferences and Section 8 on test procedures are provided.

X2.2 *Background*:

X2.2.1 Until the early 1980s, ionization damage in bipolar devices and circuits was thought to be due primarily to gain degradation in the bipolar junction transistor (BJT) and only dependent on the total dose and independent of the dose rate. Most digital circuits were thought to be hard to 1 Mrd or more; whereas, linear circuits were known to vary widely in their total dose failure levels and to often show quite different total dose response following a post irradiation thermal anneal (to remove the damage) and then reirradiated to the same total dose level.

X2.2.2 *Leakage Currents*—In the early 1980s it was shown that many types of bipolar digital circuits, using recessed field oxides for lateral isolation, exhibited severe leakage currents at total dose levels as low as 5 to 10 krd **(24-26)**. There are two potential sources for this leakage: (*a*) an inversion layer under the thick recessed oxide, across the *p*-type channel stop, between two adjacent buried layers causing leakage between components, and (*b*) an inversion layer across the base of a walled emitter NPN BJT causing collector-emitter (C-E) leakage. The former leakage path is most likely to occur under a metal stripe that is positively biased with respect to the substrate during irradiation and often results in excessive input current high (I_h) in logic gates. Excessive C-E leakage current in BJTs often leads to functional failure.

X2.2.3 *Low Dose Rate Enhancement*—In the early 1990s, it was found that the total dose induced gain degradation in some linear microcircuit BJTs was sensitive to dose rate for dose rates below about 100 rd/s **(27)**. Furthermore, the procedure contained in 8.2.2 and in MIL-STD-883, Test Method 1019, to measure failures related to interface traps, that is, irradiate to 150 % of the specification dose and perform a 168 h, 100°C anneal) actually could result in nonconservative response when compared to low dose rate irradiation of the BJTs. This observation led to a series of tests on bipolar linear circuits that showed that many part types exhibit a low dose rate sensitivity. For some parameters the degradation at dose rates of a few mrd/s can be 5 to 10 times as great as the degradation at dose rates of 50 to 300 rd/s **(28-32)**. It was confirmed for many widely used bipolar linear circuits, therefore, that established test methods using ^{60}Co did not provide a conservative estimate of a linear bipolar circuit response at low dose rates. Indeed, several studies **(29-32)** confirmed that a true dose-rate sensitivity exists for many types of linear bipolar circuits, unlike the time dependent effects ascribed to CMOS technologies. Several theories have been proposed to explain this unexpected phenomenon **(31,33-37)**. Studies are in progress to determine the process technologies and part types that manifest the low-dose-rate effect. At the present time, 18 widely used part types have demonstrated a dose rate sensitivity **(38)**. In addition, research is underway to develop cost-effective hardness-assurance test procedures using intermediate dose rates, for example, 1 to 6 rd(SiO_2)/s, that will provide a bound to the low dose rate response **(39 to 40)**. Because this is a new area of research, direction provided in this guide should be considered preliminary. The intent is to provide suggestions and recommendations to address this complex issue of determining the worst case total dose response of bipolar circuits.

X2.3 *Degradation Mechanisms*:

X2.3.1 Long-term ionization, that is steady-state total ionizing dose, effects in bipolar devices and circuits are a result of charge trapping and interface trap formation in the oxide that overlies the base-emitter junction and other dielectric layers used for passivation and isolation. These oxide layers are significantly different from the pristine gate oxide structures because of normal circuit fabrication processes, and thus, provide a total dose response different from the often studied gate oxides. Since these oxide layers often contain a very significant number of defects, by virtue of the fabrication process, hole trapping efficiencies and interface trap generation rates usually are high.

X2.3.2 *Discrete BJTs*—Discrete BJTs are defined herein to mean the JEDEC 2NXXXX type transistors, not microcircuit test chip transistors or breakouts. In discrete BJTs, the effect of the trapped positive charge is to change the surface potential (depletion and possible inversion of *p*-doped regions and accumulation of *n*-doped regions), and the effect of the interface traps is to increase the surface recombination velocity. For a given operating condition, usually defined by V_{be} and V_{ce}, there is an increase in the base current, with little or no change in the collector current **(41 to 42)**. This increase in base current results in a reduction in the dc current gain, H_{fe}, defined as I_c/I_b. If the BJTs are similar in geometry and doping densities, an NPN will degrade more than PNP because of the effects of the positive trapped charge in the base region. It is possible that in an NPN BJT the trapped positive charge could invert the *p*-type base causing a surface leakage path from emitter to collector. The base surface doping, however, usually is high enough to prevent inversion by the trapped hole density, which usually saturates with dose at value of 10^{12}–10^{13} cm^{-2} **(43)**.

X2.3.3 *Circuits*—In bipolar circuits, the increase in the base surface current, which causes the reduction in H_{fe}, still is one of the major total dose degradation mechanisms. In addition to gain degradation, the inversion of *p*-type surface regions by the trapped positive charge also can occur leading to leakage currents between *n*-type regions, which has been observed to cause failure in some digital circuits **(24,25)**.

X2.3.3.1 *Leakage Current*—There are several potential problem regions for surface leakage currents in bipolar microcircuits. For those circuits using recessed field oxide or local oxidation of silicon (LOCOS) for lateral isolation, the *p*-type channel stop doping density under the oxide, between *n*-type regions, often is only high enough to prevent inversion from positive ion contamination, for example, sodium or potassium. These regions often are inverted easily by total dose induced trapped positive charge causing leakage between components in the circuit. Inversion of these regions occurs at much lower dose when there is a positive electric field in the oxide during irradiation, such as would occur with a positively biased metal stripe over the oxide. Such failures have been observed in LSTTL (low power Shottky TTL) digital logic **(24)**. The buried layer to buried layer (BL-BL) leakage path is illustrated in Fig. X2.1 taken from Ref **(44)**. Leakage also can occur in walled emitter BJTs **(25)**, as illustrated by the C-E leakage path of X2.1. Here the base interface doping density is much lower at the sidewall than at the top surface and may be easily inverted to form a leakage path between collector and emitter. Such structures seldom are used in discrete BJTs. The C-E leakage that can occur in walled emitter BJTs can be eliminated by using a fully recessed emitter. This method, however, will impact device integration density. C-E leakage also can occur in conventional BJT technologies if a metal stripe crosses an NPN base region and is biased positively with respect to the base during irradiation.

X2.3.3.2 *Circuit BJT Gain Degradation*—Total dose induced gain degradation in BJTs was studied extensively in the

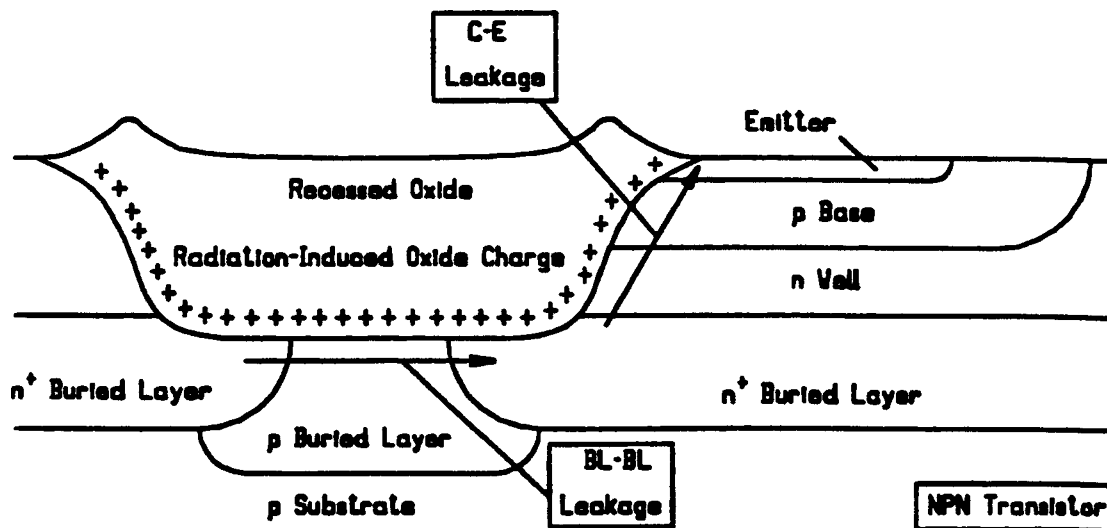


FIG. X2.1 Cross Section Showing BL-BL and C-E Leakage (Ref 44)

1960s and 1970s and a comprehensive body of knowledge concerning the degradation mechanisms exists. The recent identification of enhanced low-dose-rate sensitivity in certain types of linear bipolar circuits, however, has renewed the interest in this area.

X2.3.3.3 *NPN BJTs*—For the vertical NPN (VNPN), the ionization induced excess base current occurs in the emitter-base depletion region at the base surface (Si-SiO_2 interface) as illustrated in Fig. X2.2. The net trapped positive charge depletes the *p*-type base, extending the depletion region into the base and the interface traps increase the base surface recombination velocity. A thorough analysis using a 2-d device physics code (PISCES) has been performed on the VNPN and an analytical expression for the excess base current developed **(41)**. According to this model, the positive charge at or near the interface, consisting of the net positive trapped oxide charge and positively charged interface traps, affects the surface potential and the interface traps increase the surface recombination velocity, V_{surf}, as was previously known. The dependence of excess base current, however, ΔI_b, on the positive interface charge, N_{ox}, is of the form $\Delta I_b \propto V_{surf} \exp(N_{ox}^2)$. Because the term which involves trapped charge, N_{ox}, is exponential, the dependence of ΔI_b on dose can be superlinear. This behavior has been observed in most NPN BJTs. Once the surface potential, for higher values of N_{ox}, drives the peak of the recombination below the Si-SiO_2 interface and into the silicon, ΔI_b reaches a saturation level, which also has been observed **(43)**.

X2.3.3.4 *PNP BJTs*—Although the conventional vertical NPN BJT structure radiation response now is reasonably well understood, the radiation response of conventional lateral PNP (LPNP) and substrate PNP (SPNP) BJTs, which are used widely in bipolar linear circuits, is just beginning to be modeled in detail. These conventional LPNP and SPNP structures, shown in Fig. X2.3, often degrade at a much greater rate than conventional NPN BJTs. One reason that has been offered for the greater initial rate of degradation in the PNP BJTs is that the oxide over the emitter-base (E-B) junction in these structures usually is much thicker than in NPN BJTs **(31)**. Lateral and substrate PNPs are used widely in linear circuits but almost never used in digital circuits. A state of the art, polysilicon emitter version of the LPNP and SPNP has been characterized and modeled to understand the total dose induced degradation mechanisms **(42,45)**. The major component of the excess base current appears to be a result of increased surface recombination very near the E-B junction. This term actually is reduced

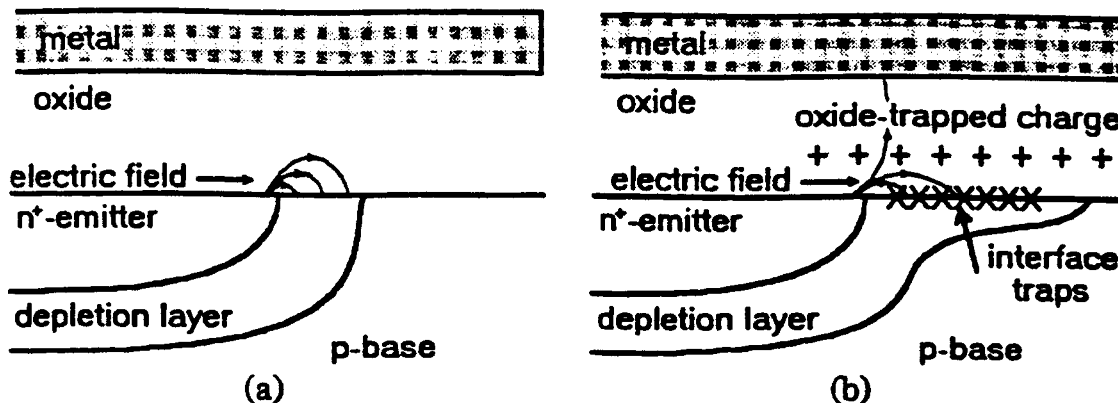


FIG. X2.2 Schematic Representation of Gain Degradation Mechanisms in an NPN BJT: (a) Preirradiation (b) Post-irradiation

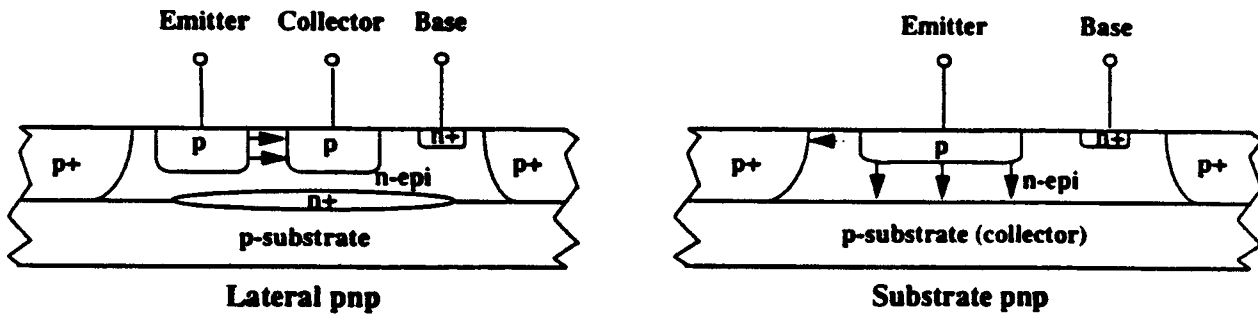


FIG. X2.3 Cross Section of Lateral and Substrate PNP Transistors Used in Many Bipolar Linear Circuits

by an increase in positive trapped charge that causes an accumulation of the *n*-type base region. For this structure, N_{ox} offsets the V_{surf} term causing a sublinear total dose dependence. In conventional LPNP and SPNP BJTs, the emitter doping density is comparable to the VNPN base doping, since the NPN base diffusion is used for the PNP emitter. The emitter doping can be as much as a factor of 100 lower than the doping in the polysilicon emitter LPNP used in the state-of-the-art process. Unpublished modeling results on the conventional LPNP structure show that the dominant mechanism may be recombination in the emitter surface region near the E-B junction, which has been depleted by the net positive charge. This base current component is similar to the base current term in VNPN BJTs. For these LPNPs, the excess base current would be expected to be superlinear with dose, rather than sublinear, as with the polysilicon emitter devices.

X2.3.3.5 *Dependence of Gain Degradation*—The magnitude of ΔI_b depends on many process, layout, irradiation, and operating parameters. These parameters have been identified and characterized extensively **(46)** for modern complementary bipolar linear microcircuit BJTs, but not as well for older circuit technologies or discretes. The irradiation conditions, which affect the magnitude of ΔI_b include dose, dose rate, temperature, and bias. Dose rate and temperature will be discussed in a later section. As previously discussed for NPNs, the dependence on dose tends to be linear at low dose, superlinear at intermediate dose, and sublinear (leading to saturation) at high dose. The range of values of "low," "intermediate," and" high," dose depend on the interface doping density in the base, the base oxide thickness, the electric field in the oxide during irradiation, and the hole trapping efficiency. The electric fields in BJT oxides often are fringing fields, resulting from junction biases. Exceptions to this are the vertical fields resulting from field plates, for example, the emitter-poly overlap in poly-emitter BJTs and intentional field plates in some lateral PNPs, and metal runs over the base that can occur in some microcircuits. Since the major components of ΔI_b occur physically near the E-B junction, they are affected most by the fringing electric field caused by V_{be}. The rate of degradation is greatest for a reverse V_{be} and smallest for a forward V_{be}. In normal circuit operation, V_{be} is forward biased at a potential between 0.1 and 0.8 *V*, depending on whether the BJT is on, off, or amplifying. In some applications, especially in linear circuits or in some BiCMOS gate outputs **(47)**, a reverse V_{be} can occur. The major layout parameters that affect ΔI_b are emitter perimeter and emitter perimeter to area ratio. This is again a result of the fact that ΔI_b physically occurs near the E-B junction at the surface, so the longer the emitter perimeter, the higher the value of ΔI_b. This is illustrated in Fig. X2.4 for a modern polysilicon emitter NPN transistor where ΔI_b is shown versus emitter perimeter to area ratio (*P/A*) for three total dose levels. The process parameters, which affect ΔI_b the most are interface doping density, oxide (dielectric) thickness, and oxide (dielectric) charge trapping efficiency. As previously implied, higher surface doping densities result in greater total dose tolerance, since the surface is harder to deplete. As stated in X2.3, bipolar oxides tend to be thicker and more highly defected than MOS oxides. Although there are well known solutions for hardening critical bipolar oxides, including the use of composite dielectrics, they are seldom used, especially in commercial technologies. Most bipolar oxides, therefore, may be considered to have very high introduction rates for both trapped positive charge and interface traps. Also, the magnitude of ΔI_b is very sensitive to operating current. The ideality factor, *n*, defined by the equation below, usually ranges between 1.5 and 2.0 depending on whether the dominant degradation mechanism is oxide trapped charge or interface traps. This causes the gain degradation to be much more severe at lower operating currents such as for V_{be} in the range of 0.5 to 0.6 *V*. This strong dependence of gain degradation on V_{be} is illustrated in Fig. X2.5.

$$\Delta I_b = \Delta I_{bs} \exp(qV_{be}/nKT) \quad \text{(X2.1)}$$

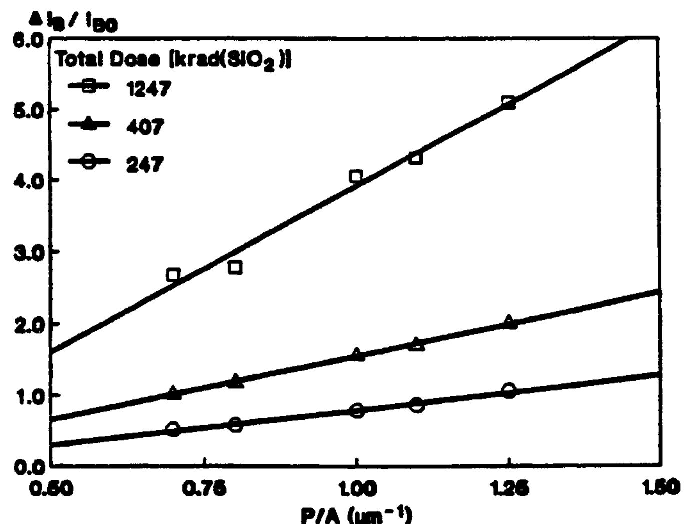


FIG. X2.4 Excess Base Current Versus Emitter Area to Perimeter Ratio for Doses of a Few Hundred Kilorads

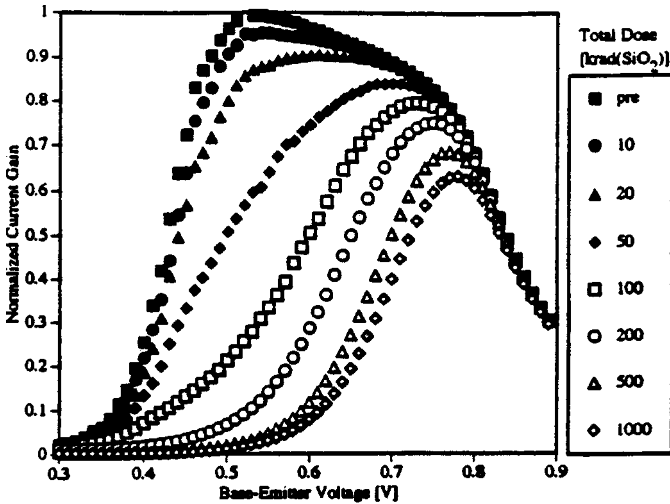


FIG. X2.5 Normalized Current Gain Versus V_{be} for Increasing Levels of Total Dose (Ref 41)

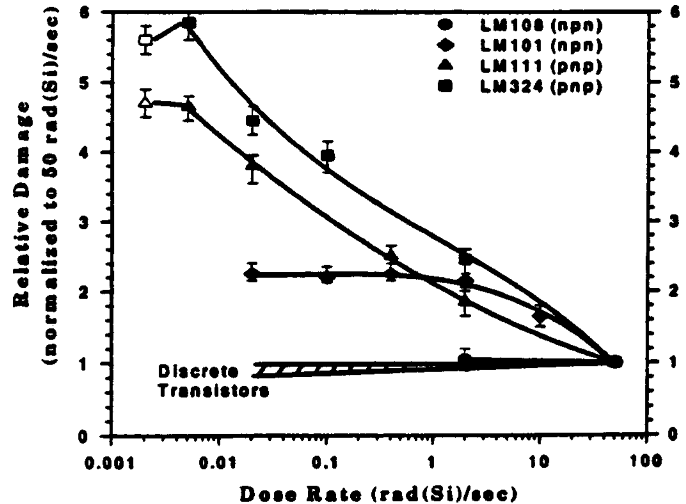


FIG. X2.6 Effect of Dose Rate on Total Dose Damage Normalized to 50 rd(Si)/s (Ref 29)

X2.3.4 *Digital Circuits*—Most digital circuits, which fail at total dose levels below 100 krd(SiO_2), fail from surface leakage currents rather than gain degradation. The exception to this failure is the integrated injection logic technology, which has almost completely disappeared from the market. This is a result of how the BJTs are used in the circuit, and the fact that only vertical NPN BJTs are used. The BJTs usually are scaled in emitter area so that they are operated at a collector current near the gain peak, for example, V_{be} = 0.7 to 0.8 V (where the degradation is least), and the forced gain to maintain saturation in the "on" state usually is between 2 and 10. The gain required to maintain a high current" on" state, therefore, would have to degrade to a very small value to pull the BJT out of saturation. Parasitic leakage currents, on the other hand, can cause parametric failure in digital circuits at total dose levels as low as 5 to 10 krd(SiO_2) **(25)**. C-E leakage in walled emitter BJTs can cause functional failure in digital circuits at total dose levels of 20 to 50 krd(SiO_2) **(26)**.

X2.3.5 *Linear Circuits and Low-Dose-Rate Enhancement*—Bipolar linear circuits usually fail from gain degradation for several reasons: (*a*) gain is a critical parameter for many of the circuit BJTs and the gain requirements for proper circuit operation often are high; (*b*) LPNP and SPNP BJTs are used extensively and are more susceptible to gain degradation than most VNPNs; and, (*c*) many linears require close matching of BJT parameters, which become unbalanced after irradiation if the BJTs are biased differently during irradiation. Because the linear circuits are quite susceptible to gain degradation failures, they are likely to exhibit the low-dose-rate sensitivity observed in microcircuit BJTs. This low-dose-rate sensitivity is more pronounced in LPNPs and SPNPs, and hence, circuits, which use these structures in critical applications, such as the input transistors of operational amplifiers and comparators or in critical current sources or mirrors, are affected by this failure mode. This is illustrated in Fig. X2.6, which shows the degradation of the input bias current at 50 krd(Si) versus dose rate (normalized to the value at 50 rd(Si)/s), for several types of operational amplifiers and comparators **(29)**. Those circuits, which use SPNPs for the input BJTs, show the greatest dose rate sensitivity. The input bias current is one of the most straightforward examples of bipolar linear circuit parameter degradation since it usually is the base current of a single input BJT. Other sensitive parameters, for example, input offset voltage, voltage gain, and slew rate of operational amplifiers and comparators and output voltage of regulators and references, are affected by the degradation of internal subcircuits using both NPN and PNP BJTs, and thus, show more complex failure mode response. The behavior of input offset voltage, V_{os}, often shows abrupt increases with dose and dose rate, making it hard to characterize and even harder to predict. An example is given in Fig. X2.7, which shows V_{os} versus dose at different dose rates for an LM324 **(31)**. The circuit mechanism for this response is thought to be the degradation of a current source using a lateral PNP BJT whose gain must degrade below

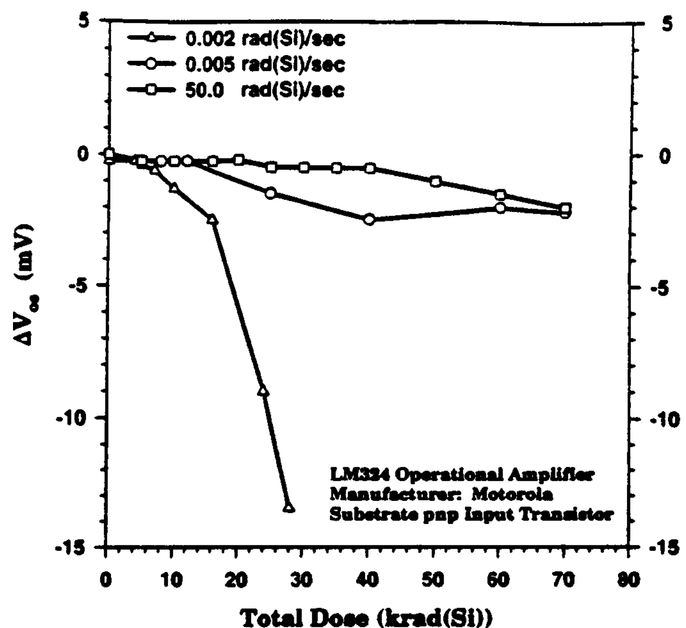


FIG. X2.7 Input Offset Voltage Versus Total Dose for LM324 at Various Dose Rates (Ref 31)

1–2 before it is no longer able to supply the proper current to a critical subcircuit. Characterization of the dose rate response of bipolar linear circuits is ongoing and will probably uncover additional complex behavior. Studies have been performed to understand the circuit mechanisms in various part types with the use of circuit simulators, for example, SPICE, and total dose and dose rate data on the various BJTs in the circuit **(30,43)**. These studies are supplemented with the use of selective irradiation of BJTs and subcircuits with a scanning electron microscope, SEM. The purpose of these studies is to demonstrate that the circuit parameter response as a function of dose and dose rate can be predicted from the dose and dose rate gain degradation of the critical BJTs. In addition to the low dose rate sensitivity, many circuits have been observed to degrade further after irradiation, during a room or even elevated temperature anneal. The degradation following anneal after a high dose rate irradiation is seldom as great as the degradation following a low dose rate irradiation **(40,48)**.

X2.3.6 *Low Dose Rate Bipolar Oxide Mechanisms*:

X2.3.6.1 The mechanism for the low dose rate sensitivity in BJTs has been studied in MOS capacitors made with BJT base oxides. It has been shown that both the net positive trapped charge density and the interface trap density are greater at dose rates below 10 rd(SiO_2)/s than at dose rates above 100 rd(SiO_2)/s **(33)**. It also has been shown that this only occurs when the externally applied electrical field is near zero. For fields above $\sim 10^4$ V/cm the low dose rate sensitivity is not observed **(35)**.

X2.3.6.2 Tests on thick MOS field oxides that have been degraded purposely with a high temperature nitrogen anneal also show the same type of behavior. It appears possible, therefore, that the low dose rate sensitivity could be seen for parasitic leakages in both bipolar and CMOS technologies. The reason that it has not been seen to date in CMOS technologies is that the first order failure will likely be a result of a path where a positive bias occurs across the oxide. In this case, the low-dose-rate sensitivity would not occur.

X2.3.6.3 There are several models that have been proposed to explain the low-dose-rate sensitivity. In the first model **(33)**, it is proposed that the effect was the result of metastable hole traps in the oxide bulk, which have trapping times at room temperature and low fields of minutes to hours. At high-dose-rate these hole traps, known as E'_δ centers, trap most of the holes near where they are created, and hold them long enough to create a space charge, which causes holes near the interface to be trapped closer to the interface, where they can be compensated by electrons from the silicon, forming border traps. At low-dose-rate, on the other hand, sufficient time is available for many of the holes trapped in the delocalized traps to become detrapped, causing less space charge. The holes trapped near the interface, hence, are further from the interface and fewer are compensated, leading to a higher net positive charge. This model was revised in 1996 **(35)** in the following manner. At high dose rate, where the irradiation time is short compared to the time for holes to be emitted from the traps and transport out of the oxide bulk, a significant space charge builds up near the center of the oxide due to metastable hole trapping. This positive space charge attracts electrons resulting in a significant number of holes in the oxide bulk being compensated. At low-dose-rates, the irradiation times are long enough for the holes to be emitted from the traps and transport out of the bulk and become trapped in deeper traps near the interface. Because there is no significant space charge in the oxide bulk, fewer are compensated by trapped electrons. The number of holes trapped, therefore, is roughly the same at high and low rates, but the number of compensating electrons trapped is greater at the higher dose rates. A property of E'_δ centers is that they release trapped holes at relatively low temperatures. The majority of these detrap at temperatures as low as 100°C, but deeper hole traps near the interface still are filled **(49)**. If one were to perform the higher-dose-rate irradiations at an elevated temperature, say 60 to 120°C, however, the results should be similar to the response at low-dose-rate. This response has been verified with extensive studies on BJTs **(36,48)** and linear circuits **(39)**.

X2.3.6.4 Another model, which was proposed in 1995 **(34)**, is that the low-dose-rate effect is due to shallow electron traps in the oxide, which again have room temperature trapping times of minutes to hours. At high-dose-rate, the electron traps are filled and capture holes, thus reducing the effective hole yield. At low rates, the electrons have time to detrap before they can capture holes, thus leading to higher trapped hole densities. One of the problems with this model is that the trapped hole densities are found to be nearly the same at high and low rates **(33,35)**.

X2.3.6.5 Also in 1995, another model was proposed to explain the low-dose-rate dependence and to explain the continued degradation of some circuits after irradiation **(31)**. This model is based on work performed in the 1970s, which showed that for low electric fields and thick oxides the hole transport time to the Si-SiO_2 interface can be minutes to hours to even days. The argument is that the effect has a longer time constant in PNPs because the oxides are thicker in lateral and substrate PNPs than in VNPNs **(31)**. This model is not a model of true dose rate response, but rather, time dependent effects. The time dependence of the hole transport cannot explain the data in Ref **(33)**, since the oxides are only 55 nm thick. It may explain some of the post-irradiation annealing behavior, however, in the lateral and substrate PNPs. Another possible explanation for the post-irradiation anneal behavior may be the slow buildup of interface traps. Work continues to be performed to refine and validate these models or develop new ones, or both.

X2.4 *Supplemental Material for Section 6—Interferences*:

X2.4.1 The areas in Section 6, which are of specific concern for bipolar technologies are bias, dose rate, TDE, and temperature.

X2.4.2 *Bias*—Total dose studies on field oxides have shown that the electric field during irradiation and during anneal have a strong influence on the damage. While a large positive electric field during irradiation is worst case for trapped positive charge, especially at high dose rate, a zero field is worst case for low dose rate enhancement. The worst case for delayed interface traps is low field during irradiation and positive field during anneal, whereas for the prompt interface traps, that have been observed in bipolar field oxides **(26,50)**,

the worst case is positive field during irradiation. A determination of the worst case irradiation and anneal bias, however, depends on the first order failure or degradation mechanism and may not be the same for all parametric circuit measurements.

X2.4.2.1 *Irradiation Bias for Discrete Transistors*—The first work on worst case irradiation bias conditions for discrete BJTs was done in the 1960s. It was shown that ΔI_b was greater for larger values of V_{ce} during irradiation. This dependence was revisited in 1994 **(29)**, in a paper that investigated the bias, dose and dose rate dependence of total dose damage in several NPN and PNP BJTs used in present day space systems. As with microcircuit BJTs the damage is greater for V_{be} of zero or reverse bias. Irradiation induced degradation also is a function of collector voltage, as was shown in the earlier studies. For certain high voltage devices **(29)**, the degradation with an irradiation bias of $V_{cb} = 50\ V$ was triple that for $V_{cb} = 10\ V$. Based on these studies, the recommended irradiation bias for discretes is $V_{be} = 0\ V$ and V_{ce} = maximum specification value, with the following exception. If the BJT is used in an application where the E-B junction is reversed biased for a significant time, for example > 5 % duty cycle, use the worst case operating reverse V_{be}.

X2.4.2.2 *Irradiation Bias for Digital Circuits*—For digital circuits the worst case bias should be determined through an analysis of the application and characterization testing. The worst case bias will depend on the failure mechanism. For parasitic leakage failures the worst case bias is the one that causes a positive oxide field in the most critical parasitic leakage path. One method to determine this condition would be to perform an analysis of the chip layout and compare it to the circuit diagram for various operating conditions. Another method would be to perform extensive characterization testing. As a general rule, the parts should be biased in a static dc condition with the maximum allowed supply voltage. The inputs should be about ½high and ½ low. The outputs should be biased as follows: (*a*) tristate outputs—tied to V_{cc}, (*b*) data latched outputs—programmed for ½high and ½low, and (*c*) sequential logic outputs—inputs set to cause ½ high and ½ low.

X2.4.2.3 *Irradiation and Anneal Bias for Linear Circuits*—The worst case irradiation and anneal bias for bipolar linear circuits may vary as a function of circuit parameter, dose rate, and temperature. Although, in theory, the worst case bias may be predicted by circuit analysis using extensive circuit BJT characterization data, often it is difficult. Some cases are relatively straightforward, for example, an operational amplifier where the most sensitive parameter is the input bias current and the input is connected only to the base of a single BJT. Most circuits designs, however, are more complex. For most circuits, the recommended approach for identifying the worst case irradiation and anneal bias is to characterize the total dose response for the full range of system operating conditions that occur for a significant fraction of the mission time. If the part is a Category B part (low-dose-rate sensitive, see 8.1.2.2), perform the worst case bias characterization test at a low enough dose rate, for example, < 1 rd(SiO_2)/s that the enhanced degradation is present. For parts where no analysis or characterization data are available, the following recommendations are given: (*a*) use a static dc configuration with a nominal supply voltage; (*b*) for operational amplifiers, use a fixed gain configuration with the differential input voltage set to force the output to a value 2 to 3 volts off the rail; (*c*) for comparators, use the maximum differential input voltage consistent with the system application; and, (*d*) for regulators and references, use the maximum input voltage consistent with the system application. In those cases where the hardness assurance tests involve an anneal, use the same anneal bias as used for irradiation.

X2.4.3 *Dose Rate*—In MOS technologies, it has been demonstrated that for dose rates below a few hundred rd/s there are no true dose rate effects, only time dependent effects. It recently has been shown that in bipolar oxides at very low electric field there are true dose rate effects that cause the degradation at low-dose-rate to be significantly higher than for the same dose delivered at high-dose-rate and followed by an anneal for a time equal to the exposure time at the low rate. To date no true dose rate effect has been verified in discrete BJTs, digital bipolar circuits or MOS devices or circuits. The effect, however, has been observed in capacitor structures at zero volts using soft MOS field oxides. For all parts, which exhibit a true dose rate effect, characterization tests should be performed at a minimum of two dose rates, including dose rates sufficiently low to observe a saturation of the degradation. Saturation of the degradation usually occurs in the range of 1–10 mrd(SiO_2)/s or higher. In some cases, testing down to saturation of degradation may be difficult or impractical to implement. This may present the tester with difficult engineering decisions.

X2.4.4 *Time Dependent Effects*—Time dependent effects are defined as those that occur as a result of the time dependence of the buildup and annealing/compensation of oxide trapped charge and interface traps. When the exposure time is short compared to the time constant of a process, most of the response occurs after irradiation. When the exposure time is comparable or long compared to the time constant of a process, however, the response occurs during the irradiation and continues after irradiation. For the case where there are no true dose rate effects, one would expect to see a similar response after a low dose rate exposure as would be seen for a high rate exposure followed by an anneal at the same bias for a period of time required to get the same dose at the low dose rate. In actual tests, the response will not be exactly the same because the response to the dose received at the end of the low-dose-rate exposure will not have had the same anneal time as for the dose received at the beginning of the low rate exposure. TDE have been characterized extensively in MOS technologies but very little in bipolar technologies. In general, very little annealing of gain degradation is observed in discrete BJTs following irradiation at either high or low rate. For bipolar digital circuits which fail as a result of parasitic leakage, there have been two reports, which show different results **(51,52)**. In one study, it was shown that the LSTTL (low power Schottky transistor-transistor logic) parts were fast annealers, and hence would fail at a much higher-dose-level as the dose rate was decreased **(51)**. In the other study, it was shown that several LSTTL circuits were very slow annealers,

and hence there was very little difference in the failure dose as a function of dose rate **(52)**. The TDE of bipolar digital circuits, which fail from C-E leakage has not been addressed.

X2.4.5 *Temperature*—The only special consideration for bipolar technologies with respect to temperature is that for Category B (low-dose-rate sensitive) parts, the degradation for higher-dose-rate irradiation at elevated temperature may be greater than at room temperature. The mechanism for this phenomenon is discussed in X2.3.5. For Category B parts, elevated temperature irradiation is recommended for characterization testing. Also, hardness assurance tests to bound the low dose rate response may include elevated temperature irradiation tests. Such tests cannot be performed in-source since the electrical measurements are to be performed at room temperature.

X2.5 *Supplemental Material for Section 8—Procedure*:

X2.5.1 Section 8 involves many tests that only apply to bipolar linear circuits. This appendix will provide supporting documentation for those test procedures that are specific to bipolar technologies.

X2.5.2 *Characterization Testing*—Characterization testing of bipolar devices and circuits with intended use dose rates of less than the baseline rate of 50 to 300 rd(SiO_2)/s (see 8.1.1.1 (*b*) (*1*) is covered in 8.1.2. There are two major parts to this characterization: a test to determine whether the part is low dose rate sensitive, and a test to determine the conditions for a hardness assurance test for dose rate sensitive parts.

X2.5.2.1 *Test for Dose Rate Sensitivity*—If the specific part type of interest (same manufacturer and process technology) already has been characterized for dose rate sensitivity, this test probably is not necessary. For example, a compendium of data on 35 to 40 part types/manufacturers recently has been published **(38)**. About half of the part types/manufacturers were found to be dose rate sensitive. Additional part types continue to be characterized. Unfortunately, there is a large variation in both the total dose and dose rate response of some part types from the same manufacturer. For example, one major bipolar linear U.S. vendor uses a different process for parts sold for mil-aero-space (MAS) application than for parts sold as commercial-off-the-shelf (COTS). The MAS parts come from a wafer bank and are processed in a different facility with a different process than the COTS parts. Dose rate tests on both MAS and COTS parts with the same part number show quite different results. Many, but not all, MAS parts are both harder and less dose rate sensitive than similar COTS parts. Because of these mixed results, it is recommended that existing data be used to classify a part as Category B (dose-rate-sensitive), but not to classify a part as Category A (not dose-rate-sensitive). Although the low-dose-rate sensitivity was first discovered in state-of-the-art bipolar microcircuit transistors, the only microcircuits that have shown enhanced low-dose-rate response have been conventional small scale linears. Only one extensive study of discrete transistors has been performed **(29)**, and in this study the dose rate response was measured only with a large C-B reverse bias. While the study did not show any enhanced low-dose-rate response, there could be an enhanced low-dose-rate response for the case of all leads shorted, as might occur for unbiased spares or for parts that are not in use for an appreciable part of a mission. Experiments are planned to look for the dose rate sensitivity of discrete BJTs with all leads shorted, but until the results are in, one may not assume that all discrete BJTs are dose rate insensitive. Most bipolar digital microcircuits, whose first order degradation mechanism is due to gain degradation, are quite hard. The one exception is integrated injection logic (I^2L). There are very few I^2L parts on the market, but they do exist, for example, the AD574 12 bit ADC. Since this part also contains linear circuitry, however, it would not be considered a strictly digital part. Bipolar digital circuits, which fail in the range of a few 10s of krd(SiO_2), usually fail as a result of leakage currents. In general, leakage current failures occur under an irradiation bias condition with a large positive electric field in the oxide. For this case, the failure mechanism is not dose rate sensitive. As a rule of thumb, one may assume that strictly digital bipolar microcircuits are Category A parts unless they contain I^2L circuitry. The sample selection for the characterization is very important. The total dose and dose rate response of bipolar linear circuits not only vary with part type (for example, an LM124 is not the same as an LM124A), manufacturer and date code, but may vary significantly from sample to sample within a date code. It is important, therefore, to have a significant sample size for the characterization test and for the sample to be representative of the parts that actually will be used in the system. The best practice is to draw the sample from the same set of parts that will be used in flight hardware. This includes ensuring that they will be the same part type, manufacturer, date code, package, and will have seen the same preconditioning, for example, burn-in. All of these factors may affect the result. The primary purpose of the dose-rate-sensitive test is to clearly establish whether a part shows enhanced low dose rate response, not whether a high-dose-rate test, with some design margin, is adequate. Because the basic mechanisms studies on the true dose rate effect have shown that elevated temperature irradiations may result in similar response as for low-dose-rate, the test for dose rate sensitivity may be performed either with a test at two dose rates or a test at a higher dose rate, say 50 to 300 rd(SiO_2)/s, at two irradiation temperatures.

X2.5.2.2 *Test at Two Dose Rates*—The test at two dose rates is based on a comparison, at a fixed dose, of the median change in the most sensitive parameter at a low dose rate compared to the median change of the same parameter at the baseline dose rate of 50 to 300 rd(SiO_2)/s (see 8.1.1.1 (*b*) (*1*). The dose levels chosen for the comparison are recommended to be logarithmically spaced (1X, 2X, 5X, 10X, etc.) up to a level 2 to 10 times the system specification level. The starting dose is arbitrary but should be low enough that the parametric changes are small (1 to 10 krd(SiO_2)). The lower dose rate value should be a factor of 1000 lower than the higher dose rate, for example, a low rate of 0.1 and a high rate of 100 rd(SiO_2)/s. If the median change at the lower rate is more than 50 % larger than the median change at the higher rate at any dose where the most sensitive parameter shows significant degradation or exceeds the preirradiation specification, or both, the part is considered dose-rate-sensitive.

X2.5.2.3 *Test at Two Irradiation Temperatures*—The test at two irradiation temperatures is based on a comparison, at a

fixed dose and dose rate, of the median change in the most sensitive parameter at an irradiation temperature of 125 ± 5°C compared to the median change of the same parameter at the baseline dose rate of 50 to 300 rd(SiO_2)/s (see 8.1.1.1 (*b*) (*1*) and an irradiation temperature of 25 ±5°C. The dose levels chosen for the comparison are recommended to be logarithmically spaced (1X, 2X, 5X, 10X, etc.) up to a level 2 to 10 times the system specification level. The starting dose is arbitrary but should be low enough that the parametric changes are small (1 to 10 krd(SiO_2)). If the median change at the higher irradiation temperature is more than 50 % larger than the median change at room temperature at any dose where the most sensitive parameter shows significant degradation or exceeds the preirradiation specification, or both, the part is considered dose-rate-sensitive.

X2.5.3 *Characterization Testing of Category B Parts*—The purpose of this test is to establish the test conditions for hardness assurance tests.

X2.5.3.1 The first part of the test is to determine the dose rate that produces the maximum parametric response at rates down to the lowest system dose rate for which a significant portion of the total mission dose is received. For example, if the system application is for a satellite in low earth orbit, where > 90 % of the dose is received while traveling through the South Atlantic Anomaly, the lowest meaningful dose rate may be on the order of 0.1 rd(SiO_2)/s. In this case, testing down to 0.001 rd(SiO_2)/s is not necessary. On the other hand, the part may be in a GEO orbit where the dose rate is reasonably constant, except for solar flare activity, and may be as low as 0.1–0.01 mrd(SiO_2)/s. In this case, it will be important to find the saturated value of the low-dose-rate enhancement. From a practical standpoint, testing below 1 mrd(SiO_2)/s (31.5 krd(SiO_2)/year) is not recommended. The response of the part should be measured at dose levels at least as high as the specification level for dose rates every decade down to the lowest system significant dose rate, but no lower than 1 mrd(SiO_2)/s and for exposure times no longer than one year. The irradiations should be performed at nominal dc static bias. Nominal should be determined by the worst case system application, if practical. It is not necessary to use unrealistic worst case bias conditions, which overdrive the part, as is often done with burn-in bias. Recommended irradiation bias conditions are discussed in X2.4.1.

X2.5.3.2 The second part of the Category B characterization testing is to find a test that will bound the low dose rate response. If the lowest system significant dose rate is on the order of 0.1 rd(SiO_2)/s, the system specification dose level is on the order of 50 krd(SiO_2) or less, then the total irradiation time to test at the system dose rate is less than a week, which may be considered practical for a lot acceptance test. In this case, a higher dose rate test may not be required; however, in most cases, it will be desirable to find a higher dose rate test to bound the low dose rate response. There are at least three approaches that may be investigated; overtest, elevated temperature irradiation, and post irradiation annealing. To date it has been shown that none of these approaches alone will be adequate to cover all part types; however, it has been demonstrated that a combination of these approaches will work for many of the very dose rate sensitive part types. Based on the mechanisms and device investigations to date, the most promising approach is the elevated temperature irradiation. Elevated temperature irradiation tests on actual circuits, however, have provided mixed results **(37,39)**. For example, as shown in Fig. X2.8, irradiation of the LM111 at 50 rd(Si)/s and 90°C does not produce much more damage than irradiation at 50 rd(Si)/s and room temperature **(37)**. If the dose rate, however, is lowered to about 1 rd(Si)/s at 90°C, the damage is enhanced greatly and is nearly the same as at very low-dose-rate. On the other hand, it was shown in another study **(39)** that if the dose rate is lowered for an elevated temperature irradiation, the total dose for which the enhancement occurs is limited, because the longer time at temperature causes annealing that offsets the effect of the enhanced degradation. There is a trade-off between dose rate and temperature, which is a function of the total dose. To determine an optimum dose rate and temperature for a given total dose would require a large matrix of test variables. Also, based on the results of the investigations to date, it is unlikely that the optimum dose rate and temperature will bound the very low dose rate response. As a starting point, it is recommended that the elevated temperature irradiation test be performed at a dose rate of 1–10 rd(SiO_2)/s and a temperature of 100±10°C. From these data, either an overtest factor or a design margin factor, or both, may be selected to bound the low-dose-rate response. This approach is illustrated in Fig. X2.9, which shows the excess input bias current versus dose for a National LM124 at several dose rates and irradiation temperatures. The low-dose-rate response is assumed to be bound by the data at 0.01 rd/s, as shown by the dotted line. If the specification level is 20 krd, then an overtest factor of 1.5 to 2.0 would suffice for a test at 1 rd/s and 100°C. For a test at 10 rd/s and 100°C, however, an overtest factor of 3 to 4 would be required. Using the design margin approach, the excess input bias current measured at 20 krd at 1 rd/s and 100°C would have to be multiplied by 1.5 to 2.0 to bound the low rate response; whereas, for a 10 rd/s at 100°C irradiation, it would have to be multiplied by 2.5 to 3.0. If the specification were 50 krd, the overtest approach would not work, even at 1 rd/s and 100°C because of saturation of the excess bias current with dose. By using the design margin approach, however, the result at 1 rd/s and 100°C only would have to be multiplied by about 1.5 to bound the low-dose-rate response. For circuits controlled by lateral or substrate PNP response, a post irradiation anneal following a high-dose-rate irradiation often will result in additional degradation **(40)**. At room temperature, the time for the additional degradation to saturate may be as long as several months, making the approach somewhat impractical. This process could be accelerated at elevated temperature, but again there will be a trade-off with the actual annealing that will occur as a result of the time at elevated temperature. Since this approach relies on time dependent effects, rather than true dose rate effects, it will not produce the same amount of damage as occurs at very low dose rate; therefore, the post-irradiation anneal approach must be combined with overtest to bound the low dose rate response. The required overtest factors often are quite high **(40)**. Based on these considerations, the post-irradiation anneal plus overtest approach is not recommended.

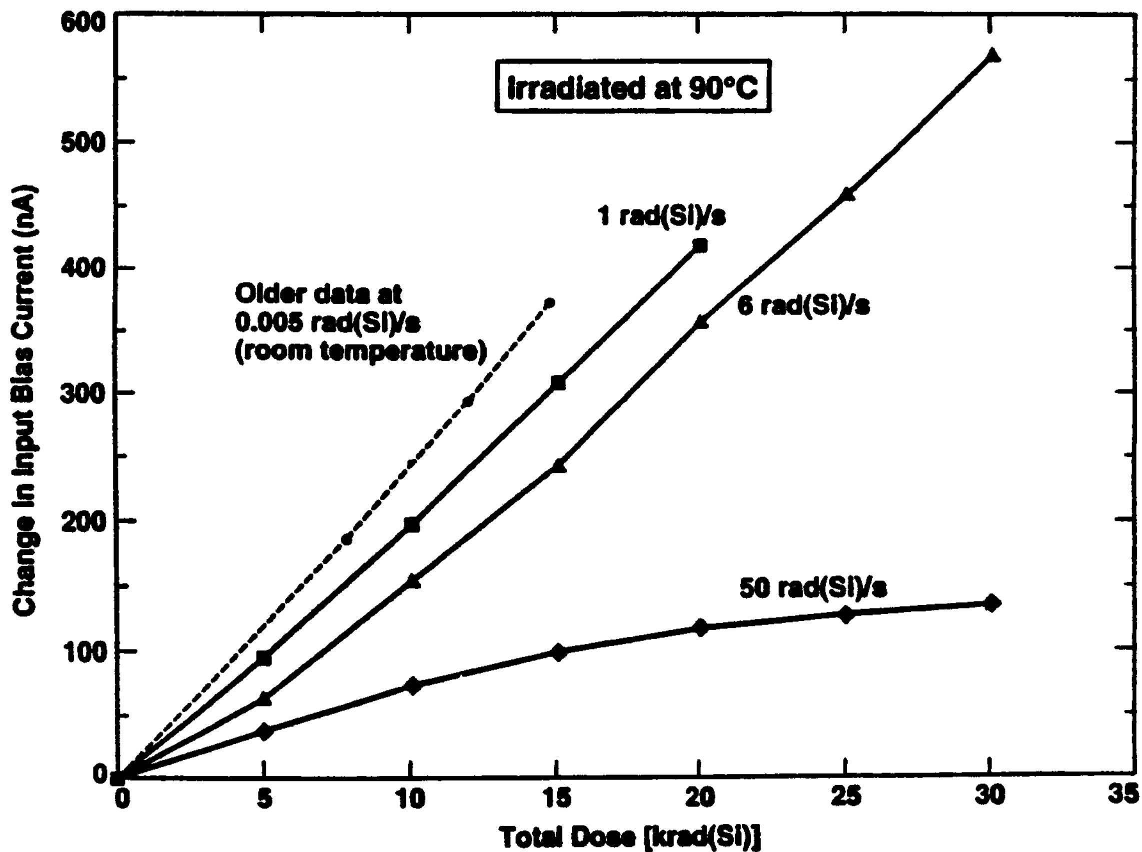


FIG. X2.8 Damage Enhancement of LM111 Input Bias Current at Various Dose Rates (Ref 37)

X2.5.4 *Hardness Assurance Testing*—The hardness assurance tests, qualification and lot acceptance, depend on whether the parts are Category A or B. For Category A parts, the testing may follow the standard tests at a dose rate of 50 to 300 rd(SiO_2)/s (see 8.1.1.1 (*b*) (*1*). For Category B (low-dose-rate sensitive) parts, there are three options. The first option (see 8.2.3.3 (*a*)) is to test at the average intended use dose rate. This option is appropriate if the total irradiation time is on the order of one month or less; hence, if the specification total dose is only 20 krd(SiO_2), dose rates as low as 10 mrd (SiO_2)/s would be practical. Caution must be used in determining the average dose rate. For many space systems, the dose rate is not constant but varies dramatically. For example, in a deep space mission, there may be years at very low-dose-rate and then a sudden increase when a planetary belt is encountered. Also, for some earth orbits, most of the dose may be accumulated when flying through the South Atlantic Anomaly. The average dose rate, therefore, should be the dose rate during the time when most of the dose is being accumulated. Option 2 (see 8.2.3.3 (*b*)) should be used if the total irradiation time under Option 1 is excessive and the part is either being used in a critical application or the response of the part is very nonlinear. The test conditions for Option 2 are determined from the characterization testing. The characterization testing is discussed under X2.5.1 (see also 8.1.2). Option 3 (see 8.2.3.3 (*c*)) may be used in those cases where the user is willing to assume some risk because the response of the part is well behaved or the application of the part is not critical. A considerable amount of engineering judgement must be used in making this decision since the amount of data to support the test conditions recommended under this option is not extensive. Under Option 3, there are two choices: test at low dose rate or test at elevated irradiation temperature. In both cases, the application of a design margin is specified. The magnitude of the specified design margin has been based on the data base currently available. A more thorough discussion of the rationale for the test conditions and caveats for Option 3 is given in reference **(53)**. The low dose rate value of 10 mrd(SiO_2)/s and the design margin of 2 for Option 3–1 is based on characterization data from about 5–7 part types. The elevated temperature irradiation conditions of 10 rd(SiO_2)/s and 100°C with a design margin of 3 for Option 3–2 is based on characterization data from 4 to 5 part types. The validity of these test conditions will be further evaluated as more data are accumulated. The conditions specified in Option 3 represent an engineering judgement based on the data available at the present time.

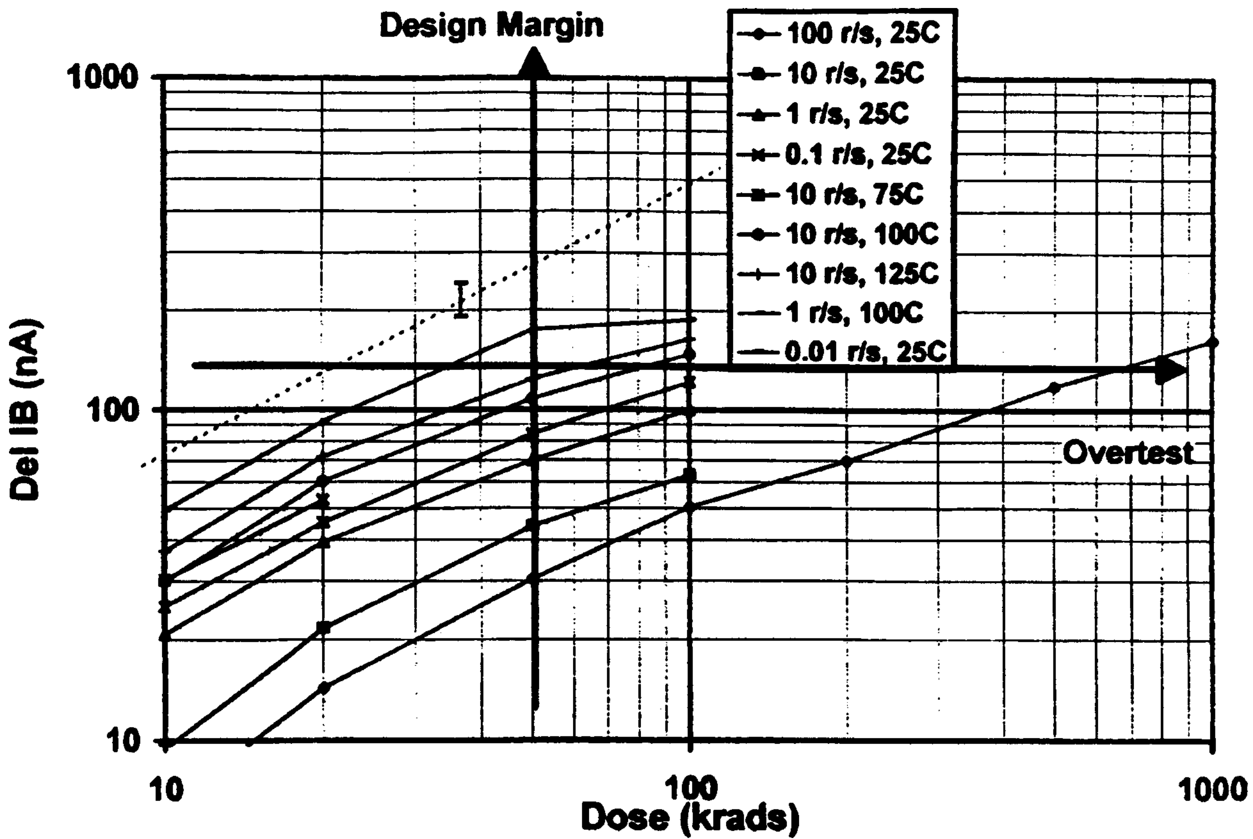


FIG. X2.9 National LM124 Excess Input Bias Current Versus Dose

X3. TOTAL DOSE TESTING FOR APPLICATION SPECIFIC INTEGRATED CIRCUITS

INTRODUCTION

Application specific integrated circuits (ASICs) are a category of digital microcircuits, which encompass a broad range of fabrication technologies, design philosophies, and functional performance. As the name implies, devices in this category are developed to perform a specific function in a system with a great deal of design input from the system developer. Typically, they have large number of input and output (I/O) terminals and operate at high clock rates. Design technologies, which are used in ASIC development include: gate arrays, standard cells, and compiled designs. They may be fabricated in a variety of silicon technologies (bipolar or CMOS), as well as gallium arsenide. The comments in this appendix are directed toward CMOS technologies since they constitute the largest market segment today.

Because ASICs are highly complex, have large I/O counts, and operate at high clock frequency, evaluation of total ionizing dose effects on their performance can be quite difficult. Typically, high performance, large pin count, automated test equipment is required to store all the test vectors and exercise the ASIC at an operational clock frequency. Few total dose irradiation facilities have such testers available, and the logistics of moving test parts between the irradiation and test facilities can be difficult within the time allotted by 8.2.2.2 (*b*) and 8.2.3.2 (*b*), (and also by MIL-STD-883, Method 1019). Understanding total dose failure mechanisms and their manifestation in ASICs, however, can result in simplified performance testing that ensures adequate characterization of total dose effects.

Total ionizing dose induced failures in ASICs are the result of radiation induced changes in transistor characteristics and the creation of leakage paths, which drastically increase supply currents, or alter the information stored as charge on critical nodes, or both. These changes are produced by a combination of mechanisms involving charge trapping and interface state generation in gate and field oxides (see Appendix X1).

In general, selection of appropriate test and measurement techniques is facilitated by detailed knowledge of the fabrication and design technology used to develop the ASIC. In particular, the

macrocell level netlist, the circuit schematics for the macrocell library, and the macrocell polygon layouts can be extremely helpful. Also, information about the total dose performance of test transistors from the fabrication technology is beneficial. Specific parameters of interest, as a function of irradiation under the conditions of Section 8, or under MIL-STD-883, Method 1019 conditions, include: (*1*) threshold voltage and mobility shifts for *N*-channel and *P*-channel gate-oxide transistors; (*2*) edge leakage for *N*-channel transistors; (*3*) field-oxide leakage between adjacent *N*-plus source/drains and *N*-plus to *N*-well regions; and (*4*) changes in macrocell propagation delay. Such information is helpful in predicting critical failure mechanisms and establishing worst case bias conditions. Models for circuit level simulation of macrocells and gate level simulation of the ASIC can be used effectively to predict performance changes as a function of total ionizing dose. If detailed design, process, and modeling information are not available, however, some general guidelines can be provided to direct the total dose testing process. The following sections provide a brief discussion of bias condition selection, test sequencing, and post-irradiation evaluation.

X3.1 *Irradiation Bias Conditions for ASICs*—The selection of irradiation bias conditions probably is the most important aspect of characterizing the total ionizing dose hardness of an ASIC. In general, consideration should be given to biasing at I/O terminals, internal state biasing for worst case timing effects, and internal state biasing for worst case leakage current effects. Typically, all of the total ionizing effects are worse for a maximum supply voltage, that is, V_{DD}. The device, therefore, should be biased at the largest V_{DD} value specified. Generally, static bias conditions produce the greatest degradation from total ionizing dose. Some technologies, however, have shown worst case response when irradiated while being actively clocked. Differences between irradiation with static versus active clocking generally are less than a factor of two. Usually, such differences are not sufficient to justify the additional test complexity associated with providing test vectors to ensure that data are being toggled through a significant portion of the ASIC by an active clock. If the ASIC design employs dynamic logic, for example, precharge/discharge read-only memory (ROM)s, an active clock may be required during irradiation. In that case, a 50 % duty cycle clock should be used with the lowest specified clock frequency.

X3.1.1 *I/O Bias Conditions*—The selection of I/O bias conditions usually is the easiest. For input terminals, the parameters, which will be affected are the I_{IL} and I_{IH} (input current for a low state and input current for a high state). They are affected typically by leakage currents associated with the input protection networks used for ESD (electrostatic discharge) suppression. There are a great variety of input protection schemes used in the semiconductor industry, and their susceptibility to total ionizing dose induced leakage depends on the type of protection elements used (diodes, resistors, FETs), the design of the protection element, and the routing of metallization and polysilicon associated with the element.

X3.1.1.1 If the test engineer has access to the design layout or to a photomicrograph of the I/O structures, he may select a bias condition that would yield the worst case leakage. He should give consideration to leakage paths under field oxide which connect V_{DD} to V_{SS} contacts and to edge leakage paths around FETs used for protection devices. In some cases, fringing fields associated with the I/O bias may play a major role in enhancing a leakage path. Where the bias voltage on the input terminal may affect several potential leakage paths, the engineer may find selection of the worst case condition to be difficult. In that case, a reasonable practice is to bias some of the input terminals to V_{DD} and others to V_{SS}. The use of current limiting resistors to connect input terminals to V_{DD} or V_{SS} is good engineering practice. In cases, where the inputs incorporate TTL to CMOS conversion circuits, the engineer must pay attention to the I/V characteristics of the terminal circuitry to ensure that he does not permit the circuit to self bias to an unintended state.

X3.1.1.2 Many ASICs use bidirectional I/O terminals to minimize the number of package pins required. In those cases, the test engineer may wish to provide input bias to some terminals and set the logic output state on others. ASIC terminals intended for connection to data buses usually contain provisions for setting a high impedance (Hi-Z) state by turning off the internal transistors driving the output. The test engineer should ensure that some terminals set in the Hi-Z state are irradiated with the output forced to V_{DD} while others are forced to V_{SS}. Usually, there are several types of I/O included on a microcircuit to meet the performance requirements of the different input and output signals. The different I/O types can be distinguished by their input capacitance ratings, their names, that is address, clock, data, etc., their functional performance, and their ESD protection rating. The test engineer must ensure that each type of I/O is tested in a worst case condition.

X3.1.2 *Internal State Biasing for Worst Case Timing Effects*—Dynamic performance parameters such as propagation delays and maximum operating frequency often are the most important metrics for ASIC performance. Total ionizing irradiation adversely can affect these parameters by altering the current drive characteristics of the MOS transistors. This changes the rate at which capacitive elements can be charged and discharged and alters the timing performance of the microcircuit. Whether the timing performance becomes faster or slower depends on the dose rate of the irradiation, the accumulated dose, and the bias conditions during irradiation. Some conditions cause the threshold voltage of *N*-channel transistors to move toward depletion mode operation, which typically increases their current drive and speeds up any circuitry with performance dependent on *N*-channel drive strength; however, the threshold voltage for *P*-channel transistors always moves further toward enhancement mode operation and cause the current drive to decrease. Furthermore, the

increase in interface states in both NMOS and PMOS transistors decreases the carrier mobility and reduces the drive strength accordingly.

X3.1.2.1 Any circuitry dependent on *P*-channel drive strength will slow down. Any circuitry dependent on *N*-channel drive strength may either speed up or slow down depending on the relative contribution of oxide trapped charge and interface state effects as determined by the total ionizing dose, dose rate, annealing time, and annealing temperature. Circuitry dependent on a balance between *N*-channel and *P*-channel drive will have its timing performance skewed. This can be important particularly for logic propagation paths, which are sensitive to race conditions, that is, precise timing of the arrival of two or more pulses to ensure proper logic performance. For example, CMOS NOR circuits tend to become faster in their high-to-low transitions because of the increased drive strength of the parallel *N*-channel transistors. They tend to become slower in their low-to-high transitions because of diminished drive strength in series connected *P*-channel. These effects become more pronounced as the fan-in of the NOR increases. CMOS NAND circuits typically do not show as much change in timing performance for equivalent dose because the *N*-channel transistors are connected in series and the *P*-channel transistors are connected in parallel. If pulses from two propagation paths must converge on a logic element simultaneously for correct logic operation, an erroneous result may occur after irradiation if one path is dominated by NOR cells and the other is dominated by NAND cells.

X3.1.2.2 If the test engineer has access to the logic schematic of the ASIC he may set irradiation bias conditions to maximize differences in timing performance. Logic states during irradiation should be selected to place most NOR cells in the low state by having all the gate inputs in a high state. Biasing of NAND cells is less critical in determining worst case performance. Worst case timing bias conditions for other cell types depends on the transistor design used to implement them and their fan-in. The use of a timing simulator and post-irradiation timing models is required to perform a quantitative design of worst case bias states for complex ASICs.

X3.1.2.3 In many cases, the test engineer may not have access to the cell schematics to determine the worst case bias conditions for all cell types. In those cases, he should select states, which place the maximum number of cells in a low-state. If he has no insight into the gate level design of the ASIC, he should pick logic states which set a 50 % mix of low states and high states on logic buses, at multiplexer outputs, in registers, and at other locations under his control.

X3.1.2.4 To mitigate problems associated with race conditions, most ASIC designs use a discipline requiring a two phase nonoverlapping clock to control the movement of data through the circuit. Typically, the clock circuit is designed carefully to ensure symmetrical operation in the high-to-low and low-to-high transitions. The clocking tree, that is, the clock distribution lines and any clock buffers) is designed to minimize any skewing of the clock signal. If the ASIC can be irradiated in a static mode, the test engineer should set the clock input so that the main clock driver cell is in the low state during irradiation. If he does not have enough insight into to design to determine how to set the state at the clock terminal, he may wish to determine the worst case condition empirically by irradiating two samples with different clock states.

X3.1.3 *Internal Biasing for Worst Case Leakage Effects*—Post-irradiation leakage current is not usually as important a parameter in ASICs as it is in memories or to some extent in microprocessors. ASICs typically are operated at a high clock rate, and their normal operating current significantly exceeds the post-irradiation leakage current. The leakage current performance, however, can provide some insight into the overall radiation hardness of the technology. Also, some ASICs contain a significant amount of memory and register files. Those devices may be placed in stand-by mode to conserve system power. In such cases, the post-irradiation current may be of significant interest.

X3.1.3.1 Since *N*-channel transistors are associated with most leakage paths, bias conditions which place a high state on the *N*-channel gate will lead to worst case leakage. In circuits, such as memory cells or latches, where data is stored in cross-coupled inverters, the engineer should ensure that a known logic state is written into the storage cell. Typically, a checkerboard pattern is stored during irradiation, and then its complement is written for the post-irradiation leakage test. This ensures that the transistors which were biased for worst case leakage are tested to determine their leakage performance.

X3.1.3.2 If the ASIC test engineer has access to cell layouts or a photomicrograph of the microcircuit, he may identify regions where field oxide leakage may be maximized. Usually, they are associated with polysilicon that crosses over adjacent well and substrate regions. Logic states which place a positive bias on those polysilicon strips enhance field oxide leakage. The bias on metallization layers usually is not of concern because there is an intervening layer of dielectric between the first level of metal and the substrate. The increased dielectric thickness reduces the field strength from the metal bias to the substrate and decreases its effect on charge trapping and subsequent substrate inversion.

X3.2 *Total Ionizing Dose Irradiation Sequence for ASICs*—Irradiation of ASIC test sample typically is performed in a sequence of exposures with electrical characterization performed after each dose step. Since oxide trapped charge and interface state buildup occur at different rates and produce different effects, the test engineer must ensure that he has sampled the ASIC performance frequently enough to detect the dose at which worst case effects occur. If the device is fabricated using an unhardened process technology, functional or parametric failure may occur at a very low total dose, that is, 1000 to 10 000 rd(Si)). The first test point for unhardened technologies, therefore, should be taken at 1 krd(Si). Subsequent tests should be performed at evenly spaced logarithmic steps. A 1-2-5-10 sequence often is used in the initial radiation characterization. Once the failure level is bracketed from these tests, additional test points can be added or shifted into the vicinity of worst case degradation to define the failure dose more precisely; however, the test engineer must be cautious about restricting data collection to an expected failure dose region, particularly where unhardened fabrication technologies

are concerned. Those technologies often exhibit a large standard deviation in the dose where their worst case degradation occurs. Enough measurement sequences must be kept in the test procedure to ensure that the failure point is not missed.

X3.2.1 During the irradiation sequence, device performance can be monitored using one or more of the following techniques:

X3.2.1.1 In-source—Measurements are made on the device while it is being actively irradiated;

X3.2.1.2 In-situ—Measurements are made at the irradiation site, but not during actual exposure to radiation; and,

X3.2.1.3 Off-site—Measurements are made using off-site test facilities typically requiring transport between the irradiation and test sites.

X3.2.2 In general, the supply current should be monitored in-source and in-situ, especially if the ASIC is being tested in a static condition or with a low-clock-rate. If a high-clock-rate is used, the operating current may mask radiation induced changes in the supply current. Radiation induced leakage under the field oxide, around transistor edges, and through the transistors themselves will be manifest in the supply current. Usually, the best procedure is to measure and record the supply current immediately prior to beginning the irradiation, monitor the current and record its peak during irradiation, and measure and record its value just after the irradiation source is turned off. This procedure provides information on the amount of annealing that is occurring between irradiation sequences. It also gives some indication of the dose at which the greatest leakage occurs, which is beneficial in selecting subsequent test sequences. The supply current is easy to monitor with an ammeter in series with the power supply.

X3.2.3 Other in-source measurements can be quite difficult to make and seldom are worth the expense and test complexity required to make them. The test engineer should keep in mind that the purpose of the test procedures such as those outlined in 8.2.2 through 8.2.2.1, 8.2.2.2, (*a*) through (*f*) or in MIL-STD-883, Method 1019, is to bound the radiation induced degradation from total ionizing dose effects where the dose may be accumulated over a broad range of dose rates. The dose rate provided by most ^{60}Co sources (50 rd(Si)/s to 300 rd(Si)/s) is unlikely to match the threat scenario for the microcircuit application; therefore, detecting a rapidly annealing failure, that is, a fault that would anneal before it could be detected by off-site measurements within an hour, through in-source testing is unlikely to provide a significantly more accurate representation of failure bound unless the environment happens to match the ^{60}Codose rate.

X3.2.4 Paragraphs 8.2.2.2 (*b*) and 8.2.3.2 (*b*) (and also MIL-STD-883, Method 1019) require electrical characterization of the part within 1 h following the exposure and initiation of the next exposure sequence within 2 h. The complexity of state-of-the-art ASICs usually necessitates the use of high performance automated test equipment to evaluate fully the functional and timing operation of the devices at their rated clock frequency. Since few irradiation sites have such equipment, the test devices often must be transported from the radiation source to the test location. During transport, the device leads should be shorted by placing them in conductive foam. Since ASICs typically are developed for specific applications, functional test instrumentation often is available, which exercises the functions most important to the system, that is, a subset of the complete set of test vectors, but does not perform an exhaustive characterization. Such instrumentation usually is adequate for detecting radiation induced failures. Although locating instrumentation at the irradiation site would simplify greatly testing logistics, any results based on an application specific tester should be verified against results from a tester capable of exercising the full suite of test vectors. Appendix X3.3 provides some guidance in selecting a subset of test vectors for on-site, post-irradiation evaluation of ASIC performance.

X3.2.5 The requirement given in 8.2.2 through 8.2.2.3 (*f*) (and also in MIL-STD-883, Method 1019), for biased, high-temperature anneal (BHTA) provides a method for bounding performance degradation resulting from interface state build-up. The device is irradiated to 150 % of its specified radiation hardness level and then subjected to a biased anneal at 100°C for 168 h and retested. The ASIC must be fully functional and pass parametric tests after the BHTA process. If an ASIC is being characterized to establish its hardness capability, samples should be removed from the test population at each step in the test sequence (for doses where significant interface state growth is possible) and subjected to BHTA to ensure that interface state effects are not the dominant failure mechanism (see X1.3.2.5).

X3.3 *Post-Irradiation Evaluation of ASICs*—Detection of radiation induced faults in the ASIC requires careful attention to the electrical characterization procedures used to evaluate parametric and functional performance following irradiation. Evaluation of those procedures should begin with consideration of the test equipment. If automated test equipment (ATE) is being used for parametric measurements, its current resolution capability should be compared with the expected preirradiation and post-irradiation current values. Some ATE systems are limited to current resolution of 100 nA. While such a capability is adequate for demonstrating that currents do not exceed specification, it may not be adequate to measure accurately actual standby supply current and leakage currents for inputs and tristated outputs. These values may be only a few nanoamps initially and the changes in their values as a function of total ionizing dose may provide valuable insight into the failure mechanisms affecting the ASIC. If adequate measurement resolution is not available in the ATE, the test engineer may wish to perform supplemental measurements with a higher resolution ammeter. As noted in X3.1, supply currents in the standby mode should be measured with any ASIC registers or memory set in the logic state complement of the irradiation condition.

X3.3.1 Consideration of loading conditions also is important for obtaining good post-irradiation characterization of the part. Output high and low voltage levels, that is, (V_{OH} and V_{OL}) should be measured at the maximum specified condition for current sourcing or sinking. If TTL input stages are used, the input noise margin parameters V_{IH} (minimum input voltage recognized as a high state) and V_{IL} (maximum input voltage recognized as a low state) should be measured under maximum

input current specifications.

X3.3.2 For propagation delay measurements, the ASIC outputs should be required to drive the maximum specified capacitive load during testing. Also, the output waveform should be monitored to ensure that voltage reflections due to impedance mismatch are not causing spurious results. This is important particularly for post-irradiation measurements where changes in threshold voltage and mobility may have caused a change in the ASIC output impedance. Typically, propagation delay measurements are not performed on all possible signal paths in the ASIC. Instead, a few, typically 2 to 10 paths with the most critical timing constraints, are identified by the ASIC designer using either a static or dynamic timing simulator. Propagation delays are measured on these critical paths which are assumed to be worst case. The test engineer should ensure that the reason for designation of these paths as critical is understood and supported by analysis. As discussed in X3.1, the irradiation bias conditions to ensure worst case degradation should be used. In addition to the critical paths identified in the timing analysis, the test engineer may wish to consider other paths that may exhibit changes that are important for assessing radiation hardness. For example, a signal path which incorporates the maximum number of logic cell types used in the design, or a path which has the greatest number of cells with worst case radiation performance, for example, maximum fan-in NORs allowed in the design, could be selected. If the ASIC includes on-chip memory, the timing associated with reading and writing should be measured.

X3.3.3 Functional testing requires the application of test vectors to the ASIC inputs and monitoring the output for correct results. Rigorous functional testing usually requires the application of many thousands of test vectors, which may take several minutes on high speed ATE; however, judicious selection of test vectors may permit adequate post-irradiation characterization in less time and with less sophisticated and expensive test equipment. Some recommendations for judiciously selecting test vectors are offered below, but before discussing them, the importance of supply voltage and test frequency in the post-irradiation characterization must be noted. The most beneficial result of the post-irradiation functional characterization is an indication of the change in the performance envelope resulting from the total dose. Since the performance envelope typically is a function of supply voltage and operating frequency, the post-irradiation functionality is best represented by a plot with axes of voltage and frequency. This graph, known as a SCHMOO plot, plots a pass or fail condition for each voltage/frequency point pair. In general, the operating frequency should cover the range from below the minimum specified value to above the maximum specified value. For ASICs using dynamic logic, total dose induced leakage ay cause failures to occur first at low operating frequency. For example, source to drain leakage in an *N*-channel pass transistor may cause the charge associated with a high state to leak away before the next clock cycle occurs; therefore, the minimum operating frequency as well as the maximum, should be included in the SCHMOO testing.

X3.3.4 Care must be exercised in setting input voltage levels when performing testing for SCHMOO characterization. Typically, the I/O pads are connected to the VDD and VSS buses through the input protection diodes. If VDD is more than a diode drop below the input, the power bus will be driven from the input pads; therefore, as the supply voltage is changed, the input voltage levels should be adjusted to ensure that V_{IL} and V_{IH} conditions are met and to prevent input protection diodes from being turned on when V is set below V_{IH}. Since each point on a SCHMOO plot requires a complete test vector cycle, the use of an abbreviated vector set will be helpful in controlling test time. As a minimum, the abbreviated set should exercise the following functions:

X3.3.4.1 Any propagation path designated as a critical timing path;

X3.3.4.2 Write cycle times for any on-chip memory;

X3.3.4.3 Read access time for on-chip memory for read cycles triggered by address transitions, memory block select, and read/write enable control lines (use a physical test patterns that gives a logic 1 in a field of 0s and a logic 0 in a field on 1s);

X3.3.4.4 Data bus transfers (both all 0s and all 1s) among all blocks on internal data buses;

X3.3.4.5 I/O data transfers including any direct memory access and interrupt handling circuitry;

X3.3.4.6 Data multiplexing with transitions from logic 0 to 1 and 1 to 0 at the multiplexer output;

X3.3.4.7 Worst case manipulation of data path blocks, that is, arithmetic logic units, multipliers, barrel shifters, etc., to produce the maximum number of internal state transitions in changing from one output state to another;

X3.3.4.8 Critical functions related to the application for which the ASIC was designed.

X3.3.4.9 Reference to the top level design documentation can be extremely helpful in selecting an abbreviated set of test vectors. Examination of the state diagram, the VHDL behavioral description, or other depictions of the relationships among functional blocks can provide insight for the development of test software to exercise the most susceptible portions of the ASIC.

X3.4 *Conclusion*—ASIC technology is advancing rapidly to take advantage of the smaller feature sizes and greater density available in state-of-the-art semiconductor processing. The resultant devices are becoming true systems on a chip, and their radiation hardness will be a major contributor to the system hardness. The radiation effects test engineer must be involved early in the design process to ensure that the performance of the device and adequate controls for facilitating radiation testing are understood. Whenever possible, formalized "design for test" approaches, such as full level sensitive scan and boundary scan, should be incorporated into the design effort. The efficiency realized in the performance of radiation testing usually is worth any additional expense of the design for test and the area consumed by the testability features.

REFERENCES

(**1**) Schwank, J. R., "Basic Mechanisms of Radiation Effects in the Natural Space Radiation Environment," *1994 IEEE NSREC Short Course*, Tucson, AZ.

(**2**) Winokur, P. S., "Total Dose Radiation Effects (from the Perspective of the Experimentalist)," *1992 IEEE NSREC Short Course*, New Orleans, LA.

(**3**) Ma, T. P. and Dressendorfer, P. V., *Ionizing Radiation Effects in MOS Devices and Circuits* (Wiley, New York, 1989), Chapter 1–7.

(**4**) Fleetwood, D. M., Winokur, P. S., Reber, R. A., Jr., Meisenheimer, T. L., Schwank, J. R., Shaneyfelt, M. R., and Riewe, L. C., "Effects of Oxide Traps, Interface Traps, and Border Traps on MOS Devices," *Journal of Applied Physics*, Vol 73, l993, p.5058.

(**5**) Galloway, K. F., Gaitan, M., and Russell, T. J., "A Simple Model for Separating Interface and Oxide Charge Effects in MOS Device Characteristics," *IEEE Trans. Nucl. Sci.*, Vol 31, l984, p.1497.

(**6**) Sexton, F. W. and Schwank, J. R., "Correlation of Radiation Effects in Transistors and ICs," *IEEE Trans. Nucl. Sci.*, Vol 32, l995, p.3975.

(**7**) Winokur, P. S., Sexton, F. W., Schwank, J. R., Fleetwood, D. M., Dressendorfer, P. V., Wrobel, T. F., and Turpin, D. C., "Total-Dose Radiation and Annealing Studies: Implications for Hardness Assurance Testing," *IEEE Trans. Nucl. Sci.*, Vol 33, l986, p.1343.

(**8**) Johnston, A. H.," Super Recovery of Total Dose Damage in MOS Devices," *IEEE Trans. Nucl. Sci.*, Vol. 31, l984, p.1427.

(**9**) Schwank, J. R., Winokur, P. S., McWhorter, P. J., Sexton, F. W., Dressendorfer, P. V., and Turpin, D. C., "Physical Mechanisms Contributing to Device Rebound," *IEEE Trans. Nucl. Sci.*, Vol 31, l984, p.1434.

(**10**) Winokur, P. S., Sexton, F. W., Hash, G. L., and Turpin, D. C., "Total-Dose Failure Mechanism of ICs in Laboratory and Space Environments," *IEEE Trans. Nucl. Sci.*, Vol 34, l987, p.1448.

(**11**) Fleetwood, D. M., Winokur, P. S., and Schwank, J. R., "Using Laboratory X-ray and Co-60 Irradiations to Predict CMOS Device Response in Strategic and Space Environments," *IEEE Trans. Nucl. Sci.*, Vol 35, l988, p.1497.

(**12**) Fleetwood, D. M., Winokur, P. S., Riewe, L. C., and Pease, R. L., "An Improved Standard Total-Dose Test for CMOS Space Electronics," *IEEE Trans. Nucl. Sci.*, Vol 36, l989, p.1963.

(**13**) Fleetwood, D. M., Winokur, P. S., and Meisenheimer, T. L., "Hardness Assurance for Low-Dose Space Applications," *IEEE Trans. Nucl. Sci.*, Vol 38, l991, p.1552.

(**14**) Sexton, F. W., Fleetwood, D. M., Aldridge, C. C., Garrett, G., Pelletier, J. C., and Gaona, J. I., Jr., "Qualifying Commercial ICs for Space Total Dose Environments," *IEEE Trans. Nucl. Sci.*, Vol 39, l992, p.1869.

(**15**) Fleetwood, D. M., Winokur, P. S., Barnes, C. E., and Shaw, D. C., "Accounting for Time Dependent Effects on CMOS Total-Dose Response in Space Environments," *Radiat. Phys. Chem.*, Vol 43, l994, p. 129.

(**16**) Fleetwood, D. M., "A First Principles Approach to Total-Dose Radiation Hardness Assurance," *l995 IEEE NSREC Short Course*, Madison, WI.

(**17**) Fleetwood, D. M., Dressendorfer, P. V., and Turpin, D. C., "A Reevaluation of Worst-Case Postirradiation Response for Hardened MOS Transistors," *IEEE Trans. Nucl. Sci.*, Vol 34, l987, p. 1178.

(**18**) Winokur, P. S., Sexton, F. W., Fleetwood, D. M., Terry, M. D., Shaneyfelt, M. R., Dressendorfer, P. V., and Schwank, J. R., "Implementing QML for Radiation Hardness Assurance," *IEEE Trans. Nucl. Sci.*, Vol 37, l990, p. 1794.

(**19**) Shaneyfelt, M. R., Winokur, P. S., Meisenheimer, T. L., Sexton, F. W., Roeske, S. B., and Knoll, M. G., "Hardness Variability in Commercial Technologies," *IEEE Trans. Nucl. Sci.*, Vol 41, l994, p. 2536.

(**20**) McGarrity, J. M., "Considerations for Hardening MOS Devices and Circuits for Low Radiation Doses," *IEEE Trans. Nucl. Sci.*, Vol 27, l980, p.1739.

(**21**) *Single Event Effects and the Space Radiation Environment*, edited by D. M. Fleetwood and R. Gaillard, *IEEE Trans. Nucl. Sci.*, Vol 43, No. 2, 1996.

(**22**) Schwank, J. R., Sexton, F. W., Fleetwood, D. M., Shaneyfelt, M. R., Hughes, K. L., and Rodgers, M. S., "Strategies for Lot Acceptance Testing Using CMOS Transistors and IC's," *IEEE Trans. Nucl. Sci.*, Vol 36, l989, p. 1971.

(**23**) Shaneyfelt, M. R., Fleetwood, D. M., Schwank, J. R., Meisenheimer, T. L., and Winokur, P. S., "Effects of Burn-In on Radiation Hardness," *IEEE Trans. Nucl. Sci.*, Vol 41, l994, p.2550.

(**24**) Pease, R. L., Turfler, R. M., Platteter, D. G., Emily, D. W. and Blice, R., "Total Dose Effects in Recessed Oxide Digital Bipolar Microcircuits," *IEEE Trans. Nucl. Sci.*, NS-30, l983, pp. 4216–4223.

(**25**) Buschbom, M. L., Jeffrey, E. N., Rhine, L. E. and Spratt, D. B., "Gamma Total Dose Effects on ALS Bipolar Oxide Sidewall Isolated Devices," *IEEE Trans. Nucl. Sci.*, NS-30, l983, pp. 4105–4109.

(**26**) Pease, R. L., Emily, D. W., and Boesch, H. E., Jr., "Total Dose Induced Hole Trapping and Interface State Generation in Bipolar Recessed Field Oxides," *IEEE Trans. Nucl. Sci.*, NS-32, l985, pp. 3946–3952.

(**27**) Enlow, E. W., Pease, R. L., Combs, W. E., Schrimpf, R. D., and Nowlin, R. N., "Response of Advanced Bipolar Processes to Ionizing Radiation," *IEEE Trans. Nucl. Sci.*, NS-38, l991, pp. 1342–1351.

(**28**) McClure, S., Pease, R. L., Will, W., and Perry, G., "Dependence of Total Dose Response of Bipolar Linear Microcircuits on Applied Dose Rate," *IEEE Trans. Nucl. Sci.*, NS-41, l994, pp. 2544–2549.

(**29**) Johnston, A. H., Swift, G. M. and Rax, B. G., "Total Dose Effects in Conventional Bipolar Transistors and Linear Integrated Circuits," *IEEE Trans. Nucl. Sci.*, NS-41, l994, pp.2427–2436.

(**30**) Beaucour, J. T., Carriere, T., Gach, A., Laxague, D. and Poirot, P., "Total Dose Effects on Negative Voltage Regulator," *IEEE Trans. Nucl. Sci.*, NS-41, l994, pp.2420–2426.

(**31**) Johnston, A. H., Rax, B. G., and Lee, C. I., "Enhanced Damage in Linear Bipolar Integrated Circuits at Low Dose Rates," *IEEE Trans. Nucl. Sci.*, NS-41, l995, pp.1650–1659.

(**32**) Carriere, T., Beaucour, J., Gach, A., Johlander, B., and Adams, L., "Dose Rate and Annealing Effects on Total Dose Response of MOS and Bipolar Circuits," *IEEE Trans. Nucl. Sci.*, NS-42, l995, pp. 1567–1574.

(**33**) Fleetwood, D. M., Kosier, S. L., Nowlin, R. N., Schrimpf, R. D., Reber, R. A., Jr., DeLaus M., Winokur, P. S., Wei, A., Combs, W. E., and Pease, R. L., "Physical Mechanism Contributing to Enhanced Bipolar Gain Degradation at Low Dose Rates," *IEEE Trans. Nucl. Sci.*, NS-41, l994, pp. 1871–1883.

(**34**) Belyakov, V. V., Pershenkov, V. S., Shalnov, A. V., Shvetzov-Shilovsky, I. N., "Use of MOS Structures for the Investigation of Low-Dose-Rate Effects in Bipolar Transistors," *IEEE Trans. Nucl. Sci.*, NS-42, 1995, pp. 1660–1666.

(**35**) Fleetwood, D. M., Riewe, L. C., Schwank, J. R., Witczak, S. C. and Schrimpf, R. D., "Radiation Effects at Low Electric Fields in Thermal, SIMOX, and Bipolar-Base Oxides," *IEEE Trans. Nucl. Sci.*, NS-43, l996, pp. 2537–2546.

(**36**) Witczak, S. C., Schrimpf, R. D., Galloway, K. R., Fleetwood, D. M., Pease, R. L., Schmidt, D. M., Combs, W. E., and Suehle, J. S., "Accelerated Tests for Bounding the Low Dose Rate Radiation Response of Lateral PNP Bipolar Junction Transistors," *IEEE Trans. Nucl. Sci.*, NS-43, l996, pp. 3151–3160.

(**37**) Johnston, A. H., Lee, C. I., and Rax, B. G., "Enhanced Damage in Bipolar Devices at Low Dose Rates: Effects at Very Low Dose Rates,"*IEEE Trans. Nucl. Sci.*, NS-43, l996, pp. 3049–3059.

(**38**) Pease, R. L., Combs, W. E., Johnston, A., Carriere, T., Poivey, C., Gach, A., and McClure, S.," A Compendium of Recent Total Dose Data on Bipolar Linear Microcircuits," *1996 IEEE Radiation Effects Data Workshop Record*, (IEEE Catalog Number 96TH8199), pp. 28–37.

(**39**) Pease, R. L., and Gehlhausen, M., "Elevated Temperature Irradiation

of Bipolar Linear Microcircuits," *IEEE Trans. Nucl. Sci.*, NS-43, l996, pp. 3161–3166.

(**40**) Cole, P. L., Emily, D., Combs, W. E., and Pease, R. L., "Post-Irradiation Degradation of Input Bias Current on Commercial Linear Bipolar Integrated Circuits", presented at the *1996 IEEE Nuclear and Space Radiation Effects Conference*, Indian Wells, CA, July 15–19, 1996.

(**41**) Kosier, S. L., Wei, A., Schrimpf, R. D., Fleetwood, D. M., DeLaus, M., Pease, R. L., and Combs, W. E., "Physically Based Comparison of Hot-Carrier-Induced and Ionizing-Radiation-Induced Degradation in BJTs," *IEEE Trans. Elect. Dev.*, Vol 42, l995, p.436.

(**42**) Schmidt, D. M., Fleetwood, D. M., Schrimpf, R. D., Pease, R. L., Graves, R. J., Johnston, G. H., Galloway, K. F., and Combs, W. E., "Comparison of Ionizing-Radiation-Induced Gain Degradation in Lateral, Substrate, and Vertical PNP BJTs," *IEEE Trans. Nucl. Sci.*, NS-42, l995, pp. 541–1549.

(**43**) Kosier, S. L., Combs, W. E., Wei, A., Schrimpf, R. D., Fleetwood, D. M., DeLaus, M., and Pease, R. L., "Bounding the Total-Dose Response of Modern Bipolar Transistors," *IEEE Trans. Nucl. Sci.*, NS-41, l994, pp.1864–1870.

(**44**) Pease, R. L., Combs, W., and Clark, S., "Long Term Ionization Response of Several BiCMOS VLSIC Technologies," *Proceedings of RADECS*, Vol 91, pp.114–118.

(**45**) Schmidt, D. M., Wu , A., Schrimpf, R. D., Fleetwood, D. M., Pease, R. L., "Modeling Ionizing Radiation Induced Gain Degradation of the Lateral PNP Bipolar Junction Transistor," *IEEE Trans. Nucl. Sci.*, NS-43, l996, pp.3032–3039.

(**46**) Nowlin, R. N., Enlow, E. W., Schrimpf, R. D., and Combs, W. E., "Trends in the Total-Dose Response of Modern Bipolar Transistors," *IEEE Trans. Nucl. Sci.*, NS-39, l992, pp.2026–2035.

(**47**) Alvarez, A. R., ed., *BiCMOS Technology and Applications*, Kluwer Academic Publishers, Boston, MA.

(**48**) Schrimpf, R. D., Graves, R. J., Schmidt, D. M., Fleetwood, D. M., Pease, R. L., Combs, W. E., and DeLaus, M., "Hardness-Assurance Issues for Lateral PNP Bipolar Junction Transistors," *IEEE Trans. Nucl. Sci.*, NS-42, l995, pp.641–1649.

(**49**) Warren, W. L., Shaneyfelt, M. R., Schwank, J. R., Fleetwood, D. M., Winokur, P. S., Devine, R. A. B., Maszara ,W. P., and McKitterick , J. B., "Paramagnetic Defect Centers in BESOI and SIMOX Buried Oxides," *IEEE Trans. Nucl. Sci.*, NS-40, l993, pp.755–1764.

(**50**) Boesch, H. E., Jr., and Taylor, T. L., "Charge and Interface State Generation in Field Oxides," *IEEE Trans. Nucl. Sci.*, NS-31, l994, pp.1273–1279.

(**51**) Schiff, D., "Prediction of Dose to Failure Versus Dose Rate for a Recessed Oxide Digital Bipolar Microcircuit," *IEEE Trans. Nucl. Sci.*, NS-34, l987, pp.1742–1744.

(**52**) Jenkins, W. C., "Dose-Rate-Independent Total Dose Failure in 54F10 Bipolar Logic Circuits," *IEEE Trans. Nucl. Sci.*, NS-39, l992, pp. l899–1902.

(**53**) Pease, R. L., Cohn, L. M., Fleetwood, D. M., Gehlhausen, M. A., Turflinger, T. L., Brown, D. B., and Johnston, A. H., "A Proposed Hardness Assurance Test Methodology for Bipolar Linear Circuits and Devices in a Space Ionizing Radiation Environment," *IEEE Trans. Nucl. Sci.*, NS-44, l997, pp. l981–1988.

The American Society for Testing and Materials takes no position respecting the validity of any patent rights asserted in connection with any item mentioned in this standard. Users of this standard are expressly advised that determination of the validity of any such patent rights, and the risk of infringement of such rights, are entirely their own responsibility.

This standard is subject to revision at any time by the responsible technical committee and must be reviewed every five years and if not revised, either reapproved or withdrawn. Your comments are invited either for revision of this standard or for additional standards and should be addressed to ASTM Headquarters. Your comments will receive careful consideration at a meeting of the responsible technical committee, which you may attend. If you feel that your comments have not received a fair hearing you should make your views known to the ASTM Committee on Standards, 100 Barr Harbor Drive, West Conshohocken, PA 19428.